TSMC 2012 Open Innovation Platform®
Ecosystem Forum
The Trusted Technology and Capacity Provider

A Platform for the CoWoS™ Reference Flow
Mentor Graphics
ABSTRACT

The first phase of 3D-IC adoption will be based on silicon interposers. Designing multi-die systems using this technology introduces new challenges for the EDA design flow.

This session will provide an overview of the key challenges of 3D-IC at the planning, optimization, implementation, verification, and test stages of the design flow. We will also describe how EDA tools are being extended to address these issues:

- Planning, assembling and optimizing interposer-based designs
- P&R support for TSV, microbumps, silicon interposer redistribution layer (RDL) and signal routing
- Multi-die integration and the need for a 3D-IC cockpit
- New extraction challenges and modeling of silicon interposers and through silicon vias (TSVs)
- Test infrastructure insertion to support test access to die test features within the package
- Testing TSVs, interposers and inter-die connections, and reusing die patterns after packaging

We will also hint at the future roadmap for IC/package co-design and the evolution to integrated IC, package and PCB design environment to enable true “vertical scaling.”
A Platform for the CoWoS™ Reference Flow

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Methodology Architect
CoWoS Implementation

- Top Die bump interface
- Package bump interface
- Bump Placement, Assignment
- TSV Insertion
- CoWoS Routing
- Ground Plane Creation
- Verification

CoWoS Reference Flow 2012
- Automatic Interposer Die Creation
- Constraint Driven Routing
- Bump Alignment Check
- Interposer Connectivity Check

Mentor Graphics®
Olympus-SoC™ Floor Plan/P&R

- Bump / Ball Assignment
- CoWoS Co-Design
- Custom Design
- PDK Library
- Bump Placement With Bump File
- Constraint Driven Routing
- TSV / uBump / Probe-Pad Routing
- Front-side Metal Routing
- Combo-bump Support

Inter-die/CoWoS Verification
(DRC/LVS/RCX)

Concurrent Analysis

- SSQ / IB / SI / STA / Thermal
- CoWoS Concurrent Analysis

Design For Test

- KGD / KGS
- for Heterogeneous Stacking

3D IC Impact on Place and Route

- Physical Implementation Considerations:
  - Floor planning → Multiple constraints drive intra- and inter-die partitions
  - CTS → Balancing complexity across dies
  - Timing Analysis → TSV characteristics and inductive effects
  - Parasitic Extraction → Impact of intra-die coupling & RLC
  - IR Drop & Thermal Analysis → Inter-die drop and thermal runaway analysis
  - Routing - 3D routing for adjacent dies

Interposer Routing Full View

- Interposer probe pad routing
- Combo-bump implementation
- Inter-die DRC/LVS check
- Bump placement considering bump spacing
- Auto-aligned block placement
- Same-signal bump group routing target
- 45 degree routing support for RDL and MB
### Interposer Routing – Micro Bump and C4

- **Silicon Interposer routing in Olympus**
- **Inputs**
  - Verilog netlist
  - Bump file
  - LEF Files
  - Routed signal nets
- **Output**
  - Routed Olympus database
  - Inter-die DRC and LVS checks within the implementation system

### Combo-Bumps Support

- Automatic recognition and routing between combo-bump pair based on distance
- Support for combo-bump stream-out in LEF and GDS
- Auto recognition and routing of MT-type bump including two metal layers

### Calibre 3D Stack Verification Solution

- Maintain standard DRC, LVS, PEX verification processes
  - Verify independent die
- Introduce 3D interface verification solution
  - Verify physical: offset, rotation, scaling, etc.
  - Trace connectivity of interposer, or die, to die
- Good for interposer and 3D configurations, analog and digital flows

- **Benefits**
  - Minimal disruption to existing verification flows
    - Support flexible stacking configurations of multiple dies
  - Maximum flexibility
    - Use different process nodes and different stacking configurations (Interposer-based and full 3D)
  - Extendibility
    - to incorporate new extraction/verification solutions
Interposer and 3D Physical Verification

- DRC: verify micro-bumps are physically aligned
- LVS: verify proper electrical connectivity through die interposer interfaces
- PEX: Extract parasitics of interconnect and BRDL
- Insert provided TSV circuit into the netlists or extract TSVs and their interactions

Issues in Extracting Interposer Parasitics

- Present solution and flow good for applications with regular layout, low density TSVs.
- Not adequate for high density, high frequency applications
- Problem with non-uniform environment around the TSVs
- Does not account for TSV interactions with other TSVs, interconnect interactions between the TSV and RDL

- Interposer metal coupling might be significant (Interposer substrate is floating)
- Hard to take into account with rule-based extraction due to semiconductor substrate and frequency dependence of couplings
- Substrate treated as
  - Dielectric (for higher frequencies)
  - Floating Metal (for lower frequencies)
- Not accurate for all frequencies of interest
- Field Solver-based solution might be needed

Mentor-Supported Modeling Approaches

- Single TSV models
  - Advantage
    - Easy to integrate into a flow; Sufficient for low density TSVs
  - Challenges
    - Not adequate for high density, high frequency applications

- Compact parameterized TSV models
  - Advantage
    - Can account for some interactions; Faster than FS
  - Challenges
    - Hard to account for all situations, to parameterize for all important variables

- Field solver-based TSV extraction
  - Advantage
    - Most accurate
  - Challenges
    - Performance; Integration

TSMC CoWoS Reference Flow 2012: PV

- Performs LVS/PEX on each die and interposer separately using Calibre nmLVS/xRC
- If LVS is clean, additional interface checking is done to ensure correctness of entire design
- Interactive debugging using Calibre RVE
- In order to run LVS on the CoWoS, bumps are identified with a PORT object but not made into nets. This allows multiple port locations with different names to coexist on the same net without causing shorts
- The port name assigned to the device so that it can be uniquely matched in the source
- Calibre xRC extracts the parasitics of the dies and CoWoS
- Calibre xRC supports insertion of provided circuit into parasitics netlist

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**Tessent® Test**

- Bump / Ball Assignment
- Custom Design
- Floorplan / APR
- Inter-die/CoWoS Verification (DRC/LVS/RCX)
- Concurrent Analysis
- Design For Test

**EDA Track**

**TSMC CoWoS Reference Flow 2012**

- **Flow effective for**
  - Interposer
  - 3D stacked die
- **Flow incorporates**
  - TestKompress pattern retargeting
  - Netlist editing with Mentor DFT tools
  - IEEE P1687 (IJTAG) for test control interface
  - Memory BIST for wideIO RAM
- **New test methods introduced**
  - Scan switch network with RPCT
  - Logic die to logic die interconnect tests
  - Logic die to memory die JEDEC-based interconnect tests
  - Contactless IO leakage test (existing capability)

**Pre-bonding Test**

- Interposer
- Die Level Test
  - Compression ATPG
  - BIST (memory, logic)
- Contactless IO Test
  - Bidi JTAG for each die IO
  - Leakage check and verify bidi operation

**Post-bonding Test: Logic-to-Logic**

- Interposer
- Interconnect Test
  - IEEE 1149.1 approach
  - Test TSVs/interposer – open & short
- Pattern Retargeting
  - Die level patterns retargeted to package
Post-bonding Test: Logic-to-RAM

**External RAM Test**
- Based on Tessent MemoryBIST
- Random data memory BIST for plug-n-play RAM support

**Logic to RAM Interconnect**
- Control JEDEC cells in RAM die
- Control logic for JEDEC on top logic die

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Path Finding and Co-Design for the Next Generation of 3D, IC Packaging

**Evaluate multiple packaging options in the context of multiple PCBs**

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3D Packaging; Off-Chip Connectivity...

- Complexity of the off-chip interconnect network
  - New structures to manage; TSV, micro-bumps
  - Excel approach to managing the off-chip interfaces is broken.
Package Level Path Finding...

What is the “right” choice/technology for your Package?
- Cost, Size, Performance, etc.
- Rapid Prototyping Required.

Path-Finding Details; Interposer
- Interposer material
  - Glass, Si, etc.
- Micro-bump size and pitch
- Number of interposer metal layers
- TSV size and pitch (dynamic)
- C4 Size and pitch (dynamic)
- Package layers
- Package pin pitch and array size

Holistic Co-Design; PCB and Path Finding

Determining the “right” solution often involves board level trade-offs...

IC ↔ Package ↔ PCB Co-Design Cockpit

- Excel
- Verilog
- VHDL
- LEF/DEF
- AIF
- OpenAccess
- GDSII

- Connectivity Management
- Rule-Based Optimization
- Library Automation

- System Level Nets
- Route Target Optimization
- Multiple Scenarios
- Board Level Interfaces (Parts)
**Summary**

- Mentor Graphics provides a robust set of tools that address the challenges of CoWoS technologies
  - Advanced place & route support
  - Industry leading verification solutions
  - Industry leading test solutions
  - Co-Design across IC, Package and PCB design domains (Future)

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