Automated Approach for Waiving Physical Verification Errors at IP

(Mentor Graphics & LSI)
ABSTRACT

Redundantly reviewing recurring errors Custom and third-party IP integration can slow down SoC verification. An automated waiver management methodology enables design and verification teams to specify and process a variety of design rule waivers, reducing debugging time and improving SoC results. This technology provides customizable control to waive errors only under certain conditions or constraints.
Automated Approach for Waiving Physical Verification Errors at IP

John Ferguson
Lead Technical Marketing Engineer, Calibre PV
Mentor Graphics Design to Silicon Division

Chuck Mayernik
Senior Engineer, Physical Verification, LSI Corporation

Jayanthi Pallinti
Senior Manager, MxS / PDK & Methodology, LSI Corporation

Chien-Ming Chiang
Senior Engineer, TSMC I/O Library Department

Agenda

- Why are waivers needed and what are the challenges?
- Introduction to Calibre Automatic Waivers
- TSMC inclusion of Calibre Automatic Waivers with 28nm IP Libraries

Calibre Automatic Waivers Flow: LSI perspective

- Q: What is Waiver Flow?
  - A: A formal hierarchical mechanism to identify and mask ‘waived’ IP-level DRC/DFM violations in a final chip level DRC run

- Why Calibre Automatic Waivers?
  - Advanced Technology Nodes have increased number of design rules
  - Functional IP designed in early technology cycle can be still used ‘as-is’ when foundry updates design rule decks
  - Enables SoC designers to focus on correcting violations outside of IP
  - MGC Calibre Automatic Waivers flow allows waivers from IP to be carried to chip level

- LSI using MGC Calibre Automatic Waivers flow for 40nm and 28nm technologies currently and will continue at advanced technology nodes
  - Before waiver flow, manual review & waiver of approved DRC/DFM violations was done in redundant phases
  - Calibre Automatic Waivers increases efficiency for DRC sign-off at chip level

Calibre Automatic Waivers Flow Current Usage

1. Identify DRC/DFM rules approved for waiver at IP level
2. Generate a waiver database containing waiver geometries & waiver acceptance criteria
3. Run final DRC using waiver database to verify results are waived properly
4. Waiver database stored and delivered with each IP for CHIP integration
5. Receive multiple waiver databases from IP developers
6. Merge multiple waiver databases
7. Include merged waiver databases in final CHIP level DRC run
Calibre Automatic Waivers:
LSI Status & Challenges

Examples LSI Designs with Calibre Automatic Waivers

<table>
<thead>
<tr>
<th>Tech.</th>
<th>Design</th>
<th>Chip or IP Waiver gds (MB)</th>
<th>Full chip/ IP (GB)</th>
<th>% Runtime change**</th>
<th># IPs in Chip*</th>
<th># IPs provided waiver gds</th>
</tr>
</thead>
<tbody>
<tr>
<td>40nm</td>
<td>A</td>
<td>6.7</td>
<td>6.6</td>
<td>+15</td>
<td>16</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>0.75</td>
<td>32</td>
<td>+23</td>
<td>60</td>
<td>29</td>
</tr>
<tr>
<td>28nm</td>
<td>D</td>
<td>1.3</td>
<td>35</td>
<td>-18</td>
<td>83</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td>E</td>
<td>2.2</td>
<td>5.4</td>
<td>-5</td>
<td>70</td>
<td>13</td>
</tr>
</tbody>
</table>

* Excludes memories & standard cells
** Increase or decrease in DRC runtime with waiver gds

- Current Status
  - At LSI, MGC Calibre Automatic Waivers is used for 40nm, 28nm technologies with plan to continue for advanced technology nodes
  - Number of IP blocks waived varies anywhere from 10 to 70
  - LSI has taped out 20+ 40nm designs & 5+ 28nm designs using Calibre Automatic Waivers
  - DRC runtime increase ~20% with waivers for 40nm; still justified since waivers are automated along with improved efficiency. 28nm runtimes decrease with waiver flow!

- Calibre Automatic Waivers Challenges
  - Implementation with standard cells is challenging due to abutment combinations
  - Coping with rule logic and name changes
  - Coping with different waiver criteria for the same rule
  - Run time performance

Introducing Calibre Automatic Waivers

3rd party IP with waivers embedded into design
Waived results automatically removed at runtime

Introducing Calibre Automatic Waivers

Rules from foundry
Waived results saved for final review
Calibre Automatic Waivers Structure

Waivers Saved in Layout
- GDSII, OASIS or Virtuoso DB
- Waiver subcell per waived rule
- Single waiver layer supports all rules

Additional Data in Text
- Waiver criteria
- User name, date, comment
- Checksums to validate consistency

Variable Waiving Shape Tolerance

Waiver Criteria
- Specifies allowed shape distortion by percent area
- Specified per rule
- Set by file or save as text with the waivers
Validating Consistency and Integrity: Calibre Automatic Waivers Checksum Validation

- Time of Waiver Generation
  - Extract Key Characteristics:
    - Waiver Shapes
    - Cell Geometries
    - Rule Derivation
    - Calibre Version
  - Append to Waiver Cells as Checksum Texts

- Time of Waiver Application
  - Re-Extract Indicated Checksums in Context
  - Compare to Checksum texts

  If Unmatched:
  - Warn
  - Warn & do not apply waivers

Special Handling for Non-Standard Rules

- Support for more than just standard DRC violations
  - Waive density results per window
  - Traditional ERC and PERC rules
  - Waiving in DFM/CFA with report cards
  - Waive by Pattern Matching

TSMC Waiving Needs for IP Deployment

**IP Provider Requirements**
- No waiving of real errors
- No flagging of waived errors
- No dependency on hierarchy
- Access to majority of users
- Ability to easily incorporate and deliver with IP
- Cannot break competing PV tool flows

TSMC Validation Process

**Rigorous Testing of Calibre Automatic Waivers**
- Waiver inclusion tested
  - DRC, LVS, DFM, PDK
  - Design flow & applications
- Tested across all tech-data
- Tested across IP
  - Stand alone and in context
- Validated Calibre’s continued performance leadership
TSMC Support for Calibre Automatic Waivers

Calibre Automatic Waivers in PDK
- Waiver layer and text layers reserved:
  - Layer 255
  - Datatypes 248-255

Calibre Automatic Waivers included with 28nm I/O Libraries
- Number of cells available with Calibre Automatic Waivers
  - >70 cells for DRC
  - >30 cells ERC
- Rules waived:
  - DRC 11
  - ERC 4

Summary

Significantly Reduce PV Debug Times
- Remove “false” errors associated with IP
- Inclusion in TSMC IO libraries eases adoption

Safe and Trusted Waiver Methodology
- In production at > 35 companies
- Hundreds of successful tape-outs
- Accuracy and performance validated by TSMC at 28nm node