Multi-Patterning Unmasked!!

David Abercrombie, DFM Program Manager for Calibre, is an expert at detailing the multifaceted impacts of multi-patterning on advanced node design and verification. For designers struggling to understand the complexity and nuances of multi-patterning, his articles and videos provide a well-lit roadmap that enables them to not only comprehend how multi-patterning will change the design process, but also how they can anticipate and mitigate the potentially unwelcome effects, such as lengthy debugging of multi-patterning errors, or unforeseen influences on timing and performance.

Double Patterning Requires a Double Take

The new double patterning solution imposes new layout, physical verification, and debug requirements on the designer. If you are a designer and you hear double patterning coming your way, it is best that you do a double take and pay close attention, or you may end up with double, double, toil and trouble...

Double Patterning: Sharing the Benefit and the Burden

At 20nm, designers will be required to purchase new double patterning software, and do additional work in the design layout and verification to enable the actual double patterning processes in the fab. Like earlier manufacturing tools, the DP checking and decomposition capability requires a whole new software engine under the hood to properly analyze the layout. But unlike the earlier layout issues, DP violations can be much more pervasive, and fixing them is mandatory, not just recommended.

Debugging Double Patterning without Getting Double Vision

One of the biggest challenges in DP design is understanding and debugging DP violation loops. Unlike DRC errors, DP errors often have multiple solutions. Of course, the problem with multiple options is that not all options are created equal—some are better choices than others. But how do you know?
To Cut or Not To Cut? That is the Double Patterning Question

Using basic DP coloring, the only way to fix an odd cycle violation is to increase the spacing between any two of the polygon pairs. Of course, adding space can cause ripple effects with other layers, and may increase the size of your layout. An alternative solution for odd cycle violations is to introduce cuts into the layout—divide one of the polygons involved in the odd cycle into two pieces, and assign alternate colors to the two pieces.

Colorblind—Colorless versus Two-Color Double Patterning Design

One key DP methodology decision is as basic as whether or not you want the designers to see colors at all—called a “colorless” design flow. The alternative is a two-color flow, in which the designer tapes out two masks, choosing one of several decomposition options. Of course, there are trade-offs with any design flow you choose, so ultimately you must decide based on what is best for your organization and which flows your foundry will support.

Anchors Away – Anchoring and Seeding in Double Pattern Design

Anchoring and seeding enable a nice tradeoff between providing designers control of coloring where they need it, and ensuring manufacturing flexibility to arbitrarily color the rest of the layout as desired. However, this capability also introduces the potential for new types of DRC violations that must be addressed by the designer before taping out the design to the fab.

Monsters, Inc.: How Do I Fix These Double Patterning Errors Anyway?

If you are trying to manually correct an odd cycle or anchor path violation, there is good news and bad news. The good news is that, unlike most traditional DRC errors, these DP errors usually have multiple solutions. The bad news is that most designers’ attempts to fix a DP violation often result in a new DP violation.
Double Patterning: Challenges and Possible Solutions in Parasitics Extraction

Litho-Etch-Litho-Etch (LELE) is the most common technique of double patterning used in 20nm technology. The unavoidable misalignment of the layout masks causes variations in coupling capacitances between the polygons that are on different masks, which in turn affects both the couplings and the total capacitances of the nets.

Why do my DP colors keep changing?

At 20nm, foundries are using several different double patterning design flows, and one of the more common flows does not actually require the design team to decompose their layers into two colors. However, there are situations in which the designer may want to know what the color assignments will be. As reasonable as this may sound, seeing the DP colors will most likely degrade debug productivity, which is a surprise to most people.

Hospital Privileges: Fixing DP Errors with Cutting and Stitching

The reality is that no matter how much you know about DP, trying to correct DP errors can be frustrating and finicky. There are times when your layout can benefit from a more surgical approach...if the “hospital” you use gives you operating privileges. The correction technique is called “cutting and stitching.” But, like anything else in a layout, there are many design rules associated with forming stitches.

Chasing Rabbits: Keeping Up With DP Rule Changes

The use of stitching can greatly reduce the number of DP decomposition violations that a designer has to resolve. However, stitching also adds significantly increased complexity—the decomposition tool must process many additional design rules to generate legal stitches and know how to use them properly during coloring. The initial challenges to automating stitch generation and layer decomposition are: 1) capturing these constraints within the syntax of the tool language, and 2) adhering to the complex combination of rules.
Between a Rock and a Hard Place: Placement-Friendly DP-Aware Cell Design

Double patterning requires a design team to make some important decisions about standard cell design methodologies, or risk running into serious placement issues down the line. Understanding why this is so and what your options are, before your design teams start doing layout, will not only help you make the best choices for your company, but also enable you to keep your DP designs moving smoothly through your design flow.

You Can't Get There From Here

DP-aware and DP-compliant automated routing is no easy task, but that doesn’t mean you can’t be successful. However, you need to expect some iteration using a sign-off verification tool like Calibre. You also must align your cell design methodology with your routing methodology in regards to DP. The more you learn, experiment, and prepare, the better off you will be. Let’s look at the interaction between decisions made at the cell design level and decisions made at the routing level.

You Ain't Seen Nothing Yet: What’s Coming for Multi-Patterning

Just when you thought you were getting used to double patterning requirements and processes, multi-patterning is now a reality. While the additional MP requirements at 16/14 nm weren’t readily visible to the designer, anyone moving to the 10 nm process node will probably need to engage in some additional multi-patterning education. The 10 nm node introduces at least two new multi-patterning techniques.

The Trouble With Triples—Part 1

Those of you currently working on 20nm or 16/14nm designs who have some experience with double patterning might think to yourself, “We figured out how to use two masks, how hard could three masks be?” Triple patterning may look innocuous from the outside, but potential chaos lies just within. Let’s start with the complexity of trying to build an EDA software algorithm for automating the decomposition (coloring) and checking of a layer using TP.

The Trouble with Triples—Part 2

What do you do when your layout can’t legally be decomposed into three colors? Triple patterning introduces even more new errors, such as diamond equivalence interactions, and debugging can be tricky, but the challenges are manageable with software that helps the designer understand the design issues. Learn how to recognize and avoid triple patterning traps.
When Order Matters

Achieving the best results from double patterning error debugging means paying attention to the order in which you address those errors. Following the suggested sequence can minimize the amount of work required to fix all DP errors, and limits the confusion of misleading results being introduced in subsequent checks.

Self-Aligned Double Patterning, Part One

It may remind you of a Rorschach test, but SADP is what’s next after LELE. Self-aligned double patterning (sometimes called sidewall-assisted double patterning) creates geometries during the wafer manufacturing by creating spacers to define the spaces around the intended shapes. SADP avoids the misalignment inherent in the LELE process, because the shapes are made from one process.

Self-Aligned Double Patterning, Part Deux

SADP masks may be difficult for humans to visualize, and even harder to explain, but understanding the basic concepts and processes is essential to determining SADP’s impact on your layout and verification flows. While it remains to be seen which approaches will be adopted by the various foundries, it’s useful to have a working knowledge of the options.

Is Multi-Patterning Good for You?

As kids, we hated hearing our parents say, “It’s good for you.” As adults, we want to buy magic pills to lose weight, and we pay other people to mow our lawns. But as much as designers might want to continue letting someone else (the foundry) pay the price of multi-patterning, that is no longer possible. Multi-patterning is now a part of the design flow, and we should actually be glad, because it means we can keep on designing ICs.

Multiple Patterns, Multiple Trade-Offs

In the end, IC design comes down to trade-offs. Make the simplest change to fix one design rule violation, and you often get a fail in one of the other rules. Some of the trade-offs that are unique to multi-patterning are obvious, but others are probably not. Most of them are decisions being made in real time at a given step in the design flow, but some interact across various points in the design flow, which means they can surprise you if you aren’t considering them throughout the design flow.
Balancing on the Color Density Tightrope

Cirque du Soleil performers make it look easy. Often, so do chip designers, like when they balance between performance optimization and leakage minimization. Competing requirements are nothing new in IC design, but multi-patterning can up the ante significantly. For example, multi-patterning creates a whole new level of density requirements, because a given design layer is actually processed as more than one mask and etch step during manufacturing. The pattern defined by each mask must not only be uniform by itself, but it must also have comparable density to the other mask(s) for that layer. While there is no “one size fits all” solution, an array of automated tool capabilities can be mixed and matched to provide the best solution in a particular application space.

Are Three Eyes Better Than Two?

Although triple patterning offers the advantage of successfully decomposing many more layout constructs, error visualization of non-decomposable constructs is much more complicated. Multiple classes of issues exist, and one type of error can trigger other types or errors. A “sifted pyramid” approach helps designers eliminate errors without triggering new ones. Learn how this new technique can help minimize error correction time and maximize designer productivity.

Case Studies in P&R Double-Patterning Debug - Part 1

There are so many intricacies to putting a full chip together that a P&R tool has a hard time accounting for every single possible condition. Every P&R and chip finishing engineer should be prepared to encounter DP-associated errors, and the challenges of determining what causes them and how best to fix them. Understanding what is happening and what the error visualization is telling you enables you to quickly and efficiently debug and correct these types of DP errors.

Case Studies in P&R Double-Patterning Debug – Part 2

David continues his expert advice to P&R and chip finishing engineers on understanding and debugging multi-patterning errors accurately and efficiently. Walking through case studies of frequently-encountered errors helps designers understand and properly deal with some of the unique and interesting situations that can occur in DP processes.
Resetting Expectations on Multi-Patterning Decomposition and Checking – Part 1

Understanding the effects, limitations, and tradeoffs of DP processes can help you relieve frustration and reset your expectations to better match what you experience when decomposing and debugging DP layouts.

Resetting Expectations on Multi-Patterning Decomposition and Checking – Part 2

Triple and quadruple patterning require a new way of thinking about and managing multi-patterning decomposition and debugging. New decomposition techniques and checking capabilities protect against endless runtimes and intractable layouts.
More Multi-Patterning Information & Assistance!

**White Papers**

**Mastering the Magic of Multi-Patterning**

Don’t have time to read all of David’s articles? This white paper presents an introduction to double patterning technology, summarizing much of the detail for a quick, yet comprehensive, overview. A great way to familiarize yourself with the unique challenges of multi-patterning, and the solutions you can bring to your design and verification flows.

**Introduction to Multi-Patterning**

If you’re just looking for a brief history of the development of multi-patterning, and a high-level overview of the technology, we suggest you start with this introductory synopsis by our expert, David Abercrombie. He’ll have you speaking the multi-patterning language in no time.

**Double Patterning for Custom Design**

Custom designers have some unique challenges when implementing multi-patterning layouts. If you are a custom designer new to double patterning layouts, this white paper will help you understand and avoid common design “gotchas,” and debug DP errors more quickly and accurately.

**FinFET and Multi-Patterning Aware Place and Route Implementation**

Physical implementation tools for advanced node designs must address multi-patterning and FinFET-aware placement. The Olympus-SoC place and route tool provides a wide range of automated capabilities that support multi-patterning requirements and processes.

**Debugging Double-Patterning Errors in Place & Route: Case Studies**

P&R and chip finishing engineers will always have some unique and interesting situations to deal with in DP layouts. This paper explores and explains a variety of DP error conditions, and presents best practices and techniques for resolving them quickly and accurately.

**When Order Matters—How to Maximize the Efficiency of DP Error Debugging**

The order in which you address DP errors can make a significant difference in the efficiency of your debug efforts. Learning the sequence of ordered DP debugging explained in this white paper can help you reduce both the time you spend analyzing and fixing DP errors and your blood pressure.
Interviews and Panels

DFM and Multi-Patterning: Experts at the Table, Part 1, Part 2, Part 3

David Abercrombie is joined by other industry experts for a discussion led by Ed Sperling of Semiconductor Engineering. What are the biggest issues facing design companies, EDA suppliers, and the foundries as the industry attempts to implement multi-patterning requirements and processes? What do we need to do to succeed?

Changes and Challenges Abound in Multi-Patterning Lithography

Jeff Dorsch, from Solid State Technology’s Semiconductor Manufacturing & Design Community, interviewed a number of experts in electronic design automation and lithography, including Mentor’s David Abercrombie, to learn about the issues associated with multi-patterning lithography.

Videos

View David’s Award-Winning DP Tutorial!

David was selected by attendee vote to receive the Customer’s Choice award for his presentation on Finding and Fixing Double Patterning Errors in 20nm Designs at TSMC’s 2012 Open Innovation Platform ecosystem event. In this presentation, David describes the new constraints that double patterning brings to the 20nm node, and how IC designers can deal with DP related design rule violations.

Multi-Patterning Tech Talks Part 1 and Part 2

Brian Bailey of Semiconductor Engineering put a camera on David and interviewed him about a number of multi-patterning issues facing design teams today. Watch and learn as David explains and illustrates a variety of multi-patterning topics, including how multi-patterning is supposed to be done, what goes wrong, and how to fix it.

Calibre How-To Video: Debugging double patterning results using Calibre RealTime

Learn how to easily debug double patterning results in Calibre RealTime by using the CTO file to assign different highlight colors to the warning and conflict ring results, and to the mask1 and mask2 output layers.
Need More Help?

Register Today for In-Depth MP Training

Calibre offers the most accurate and comprehensive multi-patterning solution available in the industry today. Now you can learn how to apply this powerful tool to your MP flow. Created in close collaboration with David Abercrombie and taught by industry experts, our course will help you understand the impact of multi-patterning on your designs, how to use Calibre tools to find and fix layout problems associated with multi-patterning compliance, and how to preemptively avoid MP issues by using an MP-aware design approach.