Perform design rule checks on boards for electromagnetic interference and signal integrity issues with HyperLynx DRC.

Overview

HyperLynx® DRC is a powerful, fast, electrical design rule checking tool that automates the verification process and helps you perform design inspection iteratively. Use it to run complex checks for problems that are not easily simulated, such as rules for traces crossing splits, vertical reference plane change, and EMI/EMC. With HyperLynx DRC, you can go far beyond the error-prone, limited-scope DRCs built into layout tools.

The built-in DRCs can be parameterized by PCB designers and hardware engineers alike, as per technology and/or corporate routing or electrical guidelines. Its intuitive Project Setup Wizard makes design setup, rule running, and design analysis easy, irrespective of experience levels. With support for layout data from Mentor and non-Mentor printed circuit board (PCB) design flows, along with ODB++ and IPC-2581 standards, HyperLynx DRC fits seamlessly into your existing PCB process.

Use the script-writing and debugging environment of the HyperLynx DRC Developer Edition to write and execute custom rules to increase coverage of design verification coverage.
What’s Included

The HyperLynx DRC Standard Edition lets you quickly and easily pinpoint trouble spots in your design that can cause potential signal integrity (SI), power integrity (PI), and electromagnetic interference and compliance (EMI/EMC) issues. Among the 46 built-in Design Rule Checks (DRCs) are ten rules for DDR compliance, ten rules for EMC compliance, and rules for relative delay and length matching and closed trace/return loop.

The HyperLynx DRC Developer Edition increases the scope of design verification with 17 additional DRCs. These include six safety rules for clearance, creepage, and regulation, three rules for analog compliance, and additional rules for general SI, such as differential pair symmetry and acute angle. In total, the Developer Edition supports 63 DRCs.

Built-in engines for geometric calculation, path finding, and net topology extraction, along with a 2D field solver, provide quick and accurate results without the need to prepare device models. With the HyperLynx DRC Developer Edition, JavaScript or VBScript can be used to access database objects using automation object models and then write and execute custom rules.

Easy Setup and Navigation

HyperLynx DRC is designed for quick and easy access to design data. A built-in Project Setup Wizard walks you through the steps for running design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Project Setup Wizard.

The scope of the checks can be defined with a specific list of design objects (e.g., power nets, capacitors) called an Object List. With a sophisticated filtering system, a specific object list with names, component values, part numbers, or any other property can be generated automatically.

In addition, the associated parameters for each rule can be edited based on technology and/or corporate guidelines.

Error Reports

Once you’ve run HyperLynx DRC, an error report such as this list of t-fork topology violations is generated from where you can cross-probe to the location of the design violation. In addition, Sharelist reports (containing the image, violation details, and coordinates) can be generated in HTML for broader team review.
Scalable Solutions

HyperLynx DRC is scalable, offering a variety of configurations to meet your needs. Use the questions in the following table to determine which product is best for you.

Supported PCB layout systems and formats include:

- Mentor Graphics PADS®, Xpedition®, and Board Station®
- Cadence Allegro®, SPECCTRA®, and OrCAD®
- Zuken CADSTAR®, Visula®, CR-3000/5000/8000 PWS, and Board Designer
- Altium® Designer
- ODB++
- IPC-2581

For more information, call or visit: https://www.mentor.com/pcb/hyperlynx/electrical-rule-check