Introduction

Xpedition® Substrate Integrator provides a graphical, rapid virtual prototyping environment tuned for the exploration and integration of heterogeneous ICs into High Density Advanced Packages (HDAP). It delivers automated co-design planning and optimization of connectivity from single or multiple ICs through interposers and package, while targeting different PCBs. Designers and architects can quickly and easily assemble complete cross-domain substrate systems and drive ball map plans and pin optimization through a rule-based methodology.

Xpedition Substrate Integrator ensures ICs, packages, and PCBs are optimized in the context of each other. This results in fewer layers and tighter control of the design process for lower-cost packages and PCBs without impacting the cost of the chip. System performance is also optimized through more-direct interconnect paths.

Xpedition Substrate Integrator supports a PCB-driven planning methodology that uses key components to influence package and die pin assignments while generating the necessary logic and physical symbols for board-level integration.

Multiple Products, Multiple Packages

A company designing smart, wireless, mobile products might want to use the same multi-core APU in several devices, such as in a tablet, a laptop, a smart phone, etc. (Figure 1). The physical constraints for each application are significantly different and the electrical constraints can also be different.
Using Xpedition Substrate Integrator, this process is efficient and takes just a fraction of the time it would take to do manually, if it could be done at all. Package configurations can be rapidly evaluated using the particular target PCB, allowing the same die to be used in the most efficient way given the end-product requirements. Optional tools enable package configurations and PCB designs to be analyzed for power and signal integrity, electromagnetic characteristics (with 3D modeling), thermal characteristics and performance, plus manufacturability. Design versions can also be compared and verified.

**Multi-Mode Connectivity Management**

The unique approach of Xpedition Substrate Integrator to cross-domain connectivity management allows design teams to capture and manage connectivity in the environment they are most comfortable with. For example, package designers can use a table-based solution while board designers use a graphical schematic to work together on the same project. For early planning and prototyping, system-level connectivity can be managed internally and remain transparent to the end user. See Figure 2.

The solution also manages signal combining (shorting) in the case of name changes from domain to domain as well as power/ground shorting.

A convenient and familiar drag-and-drop technique can also be used for ball-map planning. The multi-design project manager manages the hierarchy and relationships between domains while maintaining database integrity of the individual designs. This facilitates fast and easy data exchange with the implementation tools.

**Prototyping**

Determining the best package based on cost and performance often requires the development of a custom package definition. In some cases, this can be a simple case of ball/pin depopulation. As an example, a CPU or GPU may require a completely asymmetrical array of pins to satisfy its market needs. Shown in Figure 3, Xpedition Substrate Integrator contains powerful capabilities to dynamically add, delete, copy, move, and adjust pin pitch.

**Cross-Domain Interconnect Visualization**

Rather than managing pin assignments in multiple tabs in a spreadsheet, Xpedition Substrate Integrator displays the complete system in a single view with flight lines indicating connectivity between devices, as seen in Figure 4.

From this floor plan view, rules-based optimization can be run from any direction by signal, bus, or interface. Escape and breakout routing can be included easily in the optimization process.
Rules Engine

An easy-to-use rules interface facilitates user-defined rules for pin planning and optimization. Using the rules engine, engineers can define which pins on the package can have which signals or interfaces assigned to them. Rules can also be written to ensure that critical nets are assigned adjacent to ground nets or that corner pins will only accept the ground signal.

Figure 5 shows how rules are reflected in colors that designate which rule applies to a particular ball. Several types of rules are illustrated. For example, if data busses were not allowed on inner pins, any attempt to do so would result in an error reflected by pins turning red with the reason displayed.

2.5D/3D Stack Verification

Vertical integration, especially with heterogeneous devices, requires comprehensive assembly-level verification of the system-level packaging interfaces. Interface geometries between chip designs, including bumps, balls, through-silicon or through-interposer vias (TSVs/TIVs), and copper-to-copper bonding, must be taken into account.

In conjunction with Calibre 3DSTACK, Xpedition Substrate Integrator uniquely identifies geometries per layer per die placement in the assembly, allowing accurate checking between dies (Figure 6). With the ability to differentiate the layers of interest per individual die placement, Calibre 3DSTACK enables designers to verify the physical attributes (offset, scaling, rotation etc.) of each die, while also tracing the connectivity of the interposer or die-to-die interfaces.