Formal Verification Signoff
FormalPro-LEC

The FormalPro-LEC equivalence checker saves weeks in the verification of ASICs and ICs.

Complete Solution for Gate-Level Regression Testing of ASICs and ICs Larger than 100,000 Gates

FormalPro-LEC is the Mentor Graphics solution for gate-level regression testing of ASICs and ICs of 100,000 gates or more. FormalPro-LEC uses static formal verification techniques to prove that a design is functionally identical to its golden reference. This technique is orders of magnitude faster than traditional gate-level simulation. Designs that take days or even weeks to simulate with gate-level simulation can be verified in hours or even minutes using FormalPro-LEC. For designs greater than 100,000 gates, FormalPro-LEC is an essential verification tool in an ASIC design flow.

Gate-Level Regression Testing

Regression testing is the process of verifying that a design behaves as desired, and as previously validated, while it undergoes modification in the implementation phase. When in the RTL domain, this means re-simulating the design with hundreds or even thousands of pre-written tests to ensure that it still passes every time a modification is made. These simulations take many hours per test; however, this can be alleviated by running multiple simulations in parallel. When the design goes to the implementation process — through logic synthesis and back-end physical implementation — regression testing at the gate-level requires a different methodology. The increase in volume of data from a few thousand lines of RTL code to hundreds of thousands of interconnected cells means that simulations can take days, weeks, or even months. FormalPro-LEC is a regression testing tool that verifies that a design,
after undergoing each of the implementation steps, is functionally identical to a previously signed-off reference model. This methodology is orders of magnitude faster than simulation, ensuring that regression testing of designs at the gate-level can be performed in comparable if not faster runtimes than RTL regression tests.

Integrated Support

FormalPro-LEC provides automated setup functions for Mentor Graphics synthesis and routing tools to save time and eliminate re-runs. These commands can support passing file lists and typically load pre-defined name rules and solving parameters for the most efficient configuration. Any logic constraints or hints provided by another tool are validated with additional proofs to insure an independent verification. This includes interfaces with 3rd-party tools as well.

Integrated solvers for arithmetic and retimed circuits eliminate combinational LEC bottlenecks to improve time-to-results. An arithmetic solver proves that a bounded block of gates implements the RTL expression. A specialized sequential solver will process retimed logic which would otherwise be flagged as netlist errors causing user re-runs. An integrated ECO extraction function can aid the engineer to analyze and implement design revisions either in the RTL space or in the back-end routing stages. An ECO which is minimized by LEC can reduce the change impact to a placed and routed design, reducing change risk and time-to-tapeout.

Power Aware Verification

Accellera’s UPF power aware specification format is supported for RTL-to-gate and gate-to-gate comparisons of power specification to power implementation. Example checks include power domain register type checks and preservation of isolation buffers for power domain crossings.

Debug Tool — The Shortest Route to a Correct Design

FormalPro-LEC’s debugging capabilities dramatically reduce overall verification time by enabling engineers to identify and correct a faulty design hours or even days faster than other tools.

100% Verification Coverage

FormalPro-LEC uses static verification algorithms to guarantee verification of 100 percent of the design, independent of testbenches. Unlike simulation, which tests nothing unless directed to by a testbench, FormalPro-LEC verifies every node in the design against the reference model (unless specifically directed not to). This ensures that even the subtlest introduced errors — for example, connectivity changes in the place-and-route process that alter functional behavior — are identified and reported.

Full-Chip Verification

FormalPro-LEC’s algorithms enable full-chip designs to be verified in their entirety. As designs pass through the physical implementation process, tools often optimize the design’s hierarchy to meet timing-performance requirements. Therefore, an exact correspondence between lower-level blocks in a design is not possible. FormalPro-LEC’s full chip methodology ensures that all designs, from 100,000 gates to beyond 100 million gates, can be verified in one process, without having to manually partition the design. Fully 64-bit operating modes are employed.

FormalPro-LEC works in conjunction with Questa® Formal and Veloce® to provide a scalable digital regression testing flow.

FormalPro-LEC includes an integrated ECO extraction function.
Debug features include:

- Identifies exact location of error
- Hierarchy browser
- Schematic display: single-line and gates
- Cross probing reports to gates to RTL to schematics
- Provides difference vector for use in a simulator
- FormalEyes Hazard-checks reports unused and non-toggling gates

**Unique What-If Capability Tests**

**Design Modifications in Minutes**

Once the cause of an error has been identified, FormalPro-LEC’s unique what-if capability enables engineers to investigate design modifications within the existing verification session. When a functional difference has been reported, the user tests assumptions on how to resolve the problem using the what-if function. This capability saves hours, even days, in both debug time and the duration of iterations.

**Verification Restart**

FormalPro-LEC provides a full verification restart capability. By allowing engineers to restart the tool at any stage in the verification process, FormalPro-LEC further reduces verification time by ensuring that only the processing directly related to a design or set up change is rerun.

**Standard Language Support**

FormalPro-LEC supports standard languages including VHDL-93, 87, 2002(default), and 2008; Verilog-2001, Verilog-95, SystemVerilog 2005 and 2009; Liberty; Mentor-atpg.

**Platform Support**

FormalPro-LEC is supported on Linux® based workstations with a FPGA subset also on Windows.

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