Mentor Questa VIP

Mentor Questa® Verification IP (VIP) integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Mentor, a Siemens Business supports the leading industry-standard bus families, such as PCIe, USB, and Ethernet, as well as thousands of DRAM and FLASH memory models. Questa VIP is the industry’s only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for AMBA

AMBA® Questa VIP provides a comprehensive solution for exhaustive verification of AMBA protocol-based IP and SoC products, providing the flexibility to create and cover all possible verification scenarios. AMBA Questa VIP includes ready-to-use verification components and exhaustive stimuli to increase productivity and accelerate verification signoff.
AMBA Questa VIP Use Models

Questa VIP as Master

- Supports all channels
- Supports all protocol features
- Supports configurable address and data bus widths
- Supports sideband channels
- Extensive set of sequences in sequence library
- Exhaustive feature support for:
  - Exclusive and lock access
  - Narrow transfer
  - Unaligned address
  - Atomic transactions
- Automatic handling of reset
- Configurable master delays

Questa VIP as Slave

- Supports all channels
- Supports all protocol features
- Supports configurable address and data bus widths
- Supports sideband channels
- Backdoor access to slave memory model
- Exhaustive feature support for:
  - Exclusive and lock access
  - Narrow transfer
  - Unaligned address
  - Interleaved and out of order response
  - Atomic transactions
- Automatic handling of reset
- Configurable slave delays

Point-to-Point IP Verification

Use Model for Interconnect Verification
AMBA Questa VIP Verification Capabilities

Protocol Assertions
Built-in assertions analyze traffic for protocol adherence

Coverage
Ready-to-use cover groups
  – Transaction types
  – Transaction attributes
  – Protocol features

Out-of-the-Box Stimulus
  – Achieves full Questa VIP coverage without modifications
  – Extensive sequence library for discrete protocol features
  – Stimulus to cover protocol features
  – Error injection

Analysis Components
Scoreboards
  – Read/write operations

Performance and Latency Monitor
Various performance statistics, such as read/write channel bandwidth, latency, etc.

Loggers
Analysis ports for read/write transactions

Questa Verification IP GUI for AMBA AXI
Questa Verification IP Library

Questa VIP Testbench Architecture

For the latest product information, call us or visit: www.mentor.com/fv

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