Mentor Questa VIP

Mentor Questa® VIP (QVIP) integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Mentor, a Siemens Business, supports the leading industry-standard bus families, like PCIe, USB, and Ethernet, as well as thousands of DRAM and flash memory models. Questa VIP is the industry’s only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for DDR5 Memory

DDR5 QVIP memory models offer a comprehensive solution for exhaustive verification of DDR5 controllers, providing the flexibility to create and cover all possible verification scenarios. DDR5 QVIP memory models include ready-to-use verification components and easy-to-use memory APIs to increase productivity and accelerate verification signoff.

Questa VIP Benefits

- Architected for ease-of-use and consistency across all protocols
- Comprehensive stimulus and standard-based test suites
- Exhaustive protocol checks
- UVM based testbench with ready-to-use components like monitors, loggers, and scoreboards
- Intuitive debug with transaction viewing and tracker files at various levels

DDR5 QVIP Features

- Easy integration using memory modules
  - UVM and non-UVM testbenches
  - Single module for multiple part numbers
- Built-in analysis components
  - Protocol checkers
  - Transaction loggers
  - Performance analyzer
- Configurable command and timers using JSON files and APIs
- Memory operations (read/write/compare) using file and backdoor APIs

Supported Specifications

- JEDEC DDR5 Draft Rev0.80
**DDR5 Questa VIP Memory Models**

Packaged as Verilog module
- Multiple part number support

Supports backdoor memory APIs
Supports backdoor mode register APIs
Skip initialization capability
Configurable timers using API and JSON file
Configuration checks at runtime
Configurable command values
Support all commands
3DS stack mode
Per DRAM addressability
Post package repair (Hard PPR and Soft PPR)
2N mode
Refresh management
Support all trainings
Programmable preamble and postamble

**DDR5 QVIP Use Models**
**DDR5 Questa VIP Verification Capabilities**

**Protocol Assertions**
Built-in assertions analyze traffic for protocol adherence

**Stimulus**
Automatic response to commands

**Loggers**
Independent logger for each memory interface/channel

**Performance Analyzer**
Logs various bus performance stats
GUI based interface also present

**Configurability**
JSON based configuration
Run time set/get configuration API

**Callbacks**
Data modification callbacks
Memory event notification callbacks

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**Performance Statistics for DDR5**

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<thead>
<tr>
<th>S. No</th>
<th>Parameter</th>
<th>Description</th>
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<tr>
<td>1</td>
<td>Data Bus Utilization</td>
<td>Throughput, time for which data bus is active</td>
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<tr>
<td>2</td>
<td>Data Bus Utilization Active Time</td>
<td>Time active for which data bus is active</td>
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<tr>
<td>3</td>
<td>Bank Utilization</td>
<td>Active Time, time for which bank is active</td>
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<tr>
<td>4</td>
<td>Memory Utilization</td>
<td>Active Time, time for which memory is active</td>
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<td>Link Utilization</td>
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<td>6</td>
<td>Access Sparsity</td>
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<td>7</td>
<td>Access Efficiency</td>
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<td>8</td>
<td>Individual Comments</td>
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**Data Bus Utilization Statistics**

![Data Bus Utilization Statistics](image)

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**Questa Verification IP GUI**
**Questa Verification IP Library**

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**Flash**

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**Questa VIP Testbench Architecture**

For the latest product information, call us or visit: [www.mentor.com/fv](http://www.mentor.com/fv)

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