Mentor Questa VIP

Mentor Questa® Verification IP (VIP) integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Mentor, a Siemens Business supports the leading industry-standard bus families, such as PCIe, USB, and Ethernet, as well as thousands of DRAM and FLASH memory models. Questa VIP is the industry’s only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for Display

Display Questa VIP provides a comprehensive solution for exhaustive verification of display protocol-based IP and SoC products, providing the flexibility to create and cover all possible verification scenarios. Display Questa VIP includes ready-to-use verification components and exhaustive stimuli to increase productivity and accelerate verification signoff.

Questa VIP Benefits

- Architected for ease-of-use and consistency across all protocols
- Comprehensive stimulus and standard-based test suites
- Exhaustive protocol coverage and protocol checks
- UVM based testbench with ready-to-use components like monitors, loggers, and scoreboards
- Intuitive debug with transaction viewing and tracker files at various levels

Display Questa VIP Features

- Updated to latest protocol specification for Source and Sink
- Built-in analysis components
  - Protocol checkers
  - Transaction loggers
  - Functional coverage
- Extensive sequence library for discrete protocol features
- Constraint-randomized stimulus with support for error injection

Supported Specifications

- VESA Embedded DisplayPort (eDP) Standard, Version 1.4b, October 23, 2015
- HDCP, Mapping HDCP to DisplayPort, Revision 2.3, January 22, 2019
- HDCP (Amendment for DisplayPort), Version 1.3, Revision 1.1, January 15, 2010
- VESA DSC Standard, Version 1.2a, January 18, 2017
- HDCP, Mapping HDCP to HDMI, Revision 2.3, February 28, 2018
- HDCP, Revision 1.4, July 08, 2009
- V-by-One HS Standard, Version 1.4, December 2011
Display Questa VIP Use Models

**Questa VIP as Source**
- Supports all types of interfaces
- Supports all protocol features
- Supports multi stream transport
- Supports all data rates per lane
- Supports configurable number of lanes
- Supports internal clock data recovery
- Extensive set of sequences in sequence library
- Exhaustive feature support for:
  - DSC
  - HDCP 1.3
  - HDCP 2.3
  - FEC
  - Deep color pixel encoding formats

**Questa VIP as Sink**
- Supports all types of interfaces
- Supports all protocol features
- Supports multi stream transport
- Supports all data rates per lane
- Supports configurable number of lanes
- Supports internal clock data recovery
- Exhaustive feature support for:
  - DSC
  - HDCP 1.3
  - HDCP 2.3
  - FEC
  - Deep color pixel encoding formats

*Display Questa VIP Use Models*
Display Questa VIP Verification Capabilities

**Protocol Assertions**
Built-in assertions analyze traffic for protocol adherence

**Coverage**
Ready-to-use cover groups
- Pixel formats
- Secondary data packets
- Protocol features

**Out-of-the-Box Stimulus**
- Achieves full Questa VIP coverage without modifications
- Extensive sequence library for discrete protocol features
- Stimulus to cover protocol features
- Error injection

**Analysis Components**
Scoreboards
- Pixel data matching

**Loggers**
Analysis ports for frames and secondary data packets

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**Questa Verification IP GUI for DisplayPort**

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[www.mentor.com](http://www.mentor.com)