Mentor Questa VIP

Mentor Questa® VIP (QVIP) integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Mentor, a Siemens Business, supports the leading industry-standard bus families, like PCIe, USB, and Ethernet, as well as thousands of DRAM and FLASH memory models. Questa VIP is the industry’s only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for NVMe

NVMe QVIP is a comprehensive solution for exhaustive verification of PCIe-based IP and SoC products, providing the flexibility to create and cover all possible verification scenarios. NVMe QVIP includes ready-to-use verification components and exhaustive stimuli to increase productivity and accelerate verification signoff.

Questa VIP Benefits

■ Architected for ease-of-use and consistency across all protocols
■ Comprehensive stimulus and standard-based test suites
■ Exhaustive protocol coverage and protocol checks
■ UVM based testbench with ready-to-use components like monitors, loggers, and scoreboards
■ Intuitive debug with transaction viewing and tracker files at various levels

NVMe QVIP Features

■ Latest specification features for host and controller
■ Built-in analysis components
  – Protocol checkers
  – Transaction loggers
  – Functional coverage
  – Performance statistics
■ Feature-wise extensive stimulus
■ Constraint-randomized stimulus with support for error injection

Supported Specifications

■ NVM Express™ Revision 1.4
■ PCI Express® Base Specification Revision 4.0, Version 0.7
■ AMBA® AXI and ACE Protocol Specification (ARM® IHI0022E)
■ UNH-IOL NVMe Testing Service, Test Plan for NVMe Conformance, Version 10.0
NVMe Questa VIP Use Models

**QVIP as Controller**
- Support for PCIe, AXI transports
- Support for admin and IO commands
- Fully functional controller VIP
- Built-in memory for media
- Exhaustive feature support
  - PRP/SGL
  - Arbitration mechanisms
  - All PCIe interrupt support
  - CMB, HMB, PMR
  - Protection info
  - NVMe sets
- Automatic handling of all reset types
- Configurable delay in command processing
- Faster simulation mode with backdoor initialization

**QVIP as Host**
- Auto handshake with transport support
  - Link initialization
  - Controller discovery on PF and VF
- Complete controller initialization
- Inbuilt queue handling
  - Addition/deletion
  - Doorbell status and updates
  - Queue Read/Write
  - Backdoor access
- Built-in interrupt handling
- Built-in handling for all NVMe and transport resets
- UVM register model support for NVMe controller registers
- Backdoor initialization for host QVIP
- Configurable delay in each step of command execution
NVMe Questa VIP Verification Capabilities

Protocol Assertions
Built-in assertions analyze traffic for protocol adherence

Coverage
Ready-to-use cover groups
- Admin and IO commands
- Queue management
- Crosses for commands and possible completion status

Stimulus
Out-of-the-box stimulus
- To achieve QVIP delivered coverage
- Detailed scenario wise stimulus
- Stimulus to cover state transition and protocol packets
- Error injection

Analysis Components
Scoreboards
- Scoreboard NVM media
- Read/Write operations

Performance and latency monitor
- Various performance stats like IOPS, throughput etc …
- Latency between each command operation

Loggers
Analysis ports for NVMe commands

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**Questa Verification IP GUI**
Questa Verification IP Library

Questa VIP Testbench Architecture

For the latest product information, call us or visit: www.mentor.com/fv

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