Mentor Questa VIP

Mentor Questa® VIP (QVIP) integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Mentor, a Siemens Business, supports the leading industry-standard bus families, like PCIe, USB, and Ethernet, as well as thousands of DRAM and FLASH memory models. Questa VIP is the industry’s only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for PCIe

PCIe QVIP is a comprehensive solution for exhaustive verification of PCIe-based IP and SoC products, providing the flexibility to create and cover all possible verification scenarios. PCIe QVIP includes ready-to-use verification components and exhaustive stimuli to increase productivity and accelerate verification signoff.

Questa VIP Benefits

- Architected for ease-of-use and consistency across all protocols
- Comprehensive stimulus and standard-based test suites
- Exhaustive protocol coverage and protocol checks
- UVM based testbench with ready-to-use components like monitors, loggers, and scoreboards
- Intuitive debug with transaction viewing and tracker files at various levels

Questa VIP for PCIe Features

- Latest specification and feature support for PCIe 5.0
- Comprehensive verification solution for all PCIe based devices: RC, RP, EP, switch, and retimer
- Built-in analysis components
  - Protocol checkers
  - Transaction loggers
  - Functional coverage
  - Performance statistics
- Extensive stimulus for verification of each PCIe layer

Supported Specifications

- PCI Express® Base Specification Revision 5.0, Version 1.0
- PCI Express Test Spec Link and Transaction Layer Revision 3.0, Version 0.5
- PHY Interface for PCI Express (PIPE), Version 5.0

www.mentor.com/fv
PCle Questa VIP Feature Support

Link Speed
32, 16, 8, 5, and 2.5 Gts

Verification Support
Endpoint (native and legacy)
Root complex
Switches and bridges
Retimer
PHY

Advanced Protocol Features
Precoding
Alternate protocol support
10-bit tag support
Lane margening
Framing errors
All PM states, including L1-PM
Interrupts (PIN, MSI, and MSI-X)
SRIS and SRNS
DPC, ACS, LTR, OBFF, etc.

Link Training
Crosslink, lane reversal, skew/deskew, CDR, and polarity inversion

Interface Support
PIPE
Serial

Multi-Function Support
ARI
SRIOV

Equalization
Autonomous and software controlled
Equalization bypass mode

Complete Configuration Space with 5.0 Extended Capabilities
PCIe QVIP Verification Capabilities

Protocol Assertions
Built-in assertions ensure protocol adherence
- DUT configurations
- LTSSM transitions
- TL/DL/PL packets

Coverage
Ready-to-use cover groups
- TL/DL/PL packets
- LTSSM transitions
- TS-OS fields

Callbacks
Complete control of packet fields on TX and RX paths of QVIP
- Tap TL/DL/PL packets on different layers
- Drop or modify received packets
- Insert error or delay

Stimulus
Out-of-the-box stimulus
- Sequence as per PCI-SIG compliance document
- Complete fabric enumeration
- Extensive layer-wise stimulus
- Error injection

Analysis Components
Scoreboards (PCIe memory)
- Read/write operations

Performance and latency monitors
- Various performance stats; such as throughput and bus utilization
- Packet statistics

Loggers
Analysis ports for all packets

Questa Verification IP GUI
Questa Verification IP Library

Questa VIP Testbench Architecture

For the latest product information, call us or visit: www.mentor.com/fv