Pyxis Layout Suite
Explore the Possibilities

A TOTAL DESIGN SOLUTION

Integrated circuit design is becoming more complex every day. This is especially true in analog and mixed-signal design. To address critical time-to-market issues as designs become increasingly complex, Mentor Graphics offers the Pyxis® Custom IC Design Platform, a complete IC design flow, from design capture to physical layout and verification. With the help of foundry partners, design kits are available for your target process technology, ensuring immediate access to essential data. Analog/mixed-signal IC designers who need a total design solution choose the Mentor Graphics Pyxis Custom IC Design Platform.

ANALOG/MIXED SIGNAL IC DESIGN

The solutions in the Mentor Graphics Pyxis Layout Suite offer easily configured, affordable options for design engineers who need increased productivity and an immediate, automated way of handling the physical layout of their AMS designs. Design engineers can be fully functional with the Pyxis tools in as little as one day. The Pyxis Layout Suite consists of two application bundles: Pyxis Layout and Pyxis Implement.

Key Benefits

- Improves layout design throughput up to 50X compared to manual layout methods.
- Optional products can drive productivity to even higher levels.
- Multiple tools support increasing levels of layout automation.
- Reduces DRC debugging cycles, leading to shortened time-to-market.
- Verifies DRC and LVS correctness throughout the layout process, without adding complicated steps.
- Creates DRC/LVS–correct complex layout with a simple command to improve reliability of the final product.
- Enables changes to layout based on updates to the schematic at any point in the design cycle.

Key Features

- Schematic and/or SPICE netlist driven layout flow.
- Single environment for all design tasks including: floorplanning, layout, chip assemble, and tapeout.
- Integrated Calibre® nmDRC and nmLVS for checking within the layout editor.
- Ready-to-use parameterized device generators for digital and analog layout design.
- Integrated ECO component.
- Design data interchange using OpenAccess, LEF/DEF, and GDS.

The Pyxis Layout Suite provides the physical layout component of the Mentor Graphics Pyxis Custom IC Design Platform. This suite includes application bundles for floorplanning, editing, schematic-driven layout, chip assemble, and custom routing.
These bundles are offered in a standard configuration, with optional applications that provide increasing levels of automation and functionality to address the designers unique requirements. And with Mentor Graphics, engineers can be assured they will receive the highest level of support, training, and technical assistance.

**PYXIS LAYOUT**

Pyxis Layout supports an extensive set of editing functions for efficient, accurate polygon editing. This gives the engineer full control of circuit density and performance, while improving productivity by as much as 5X to help meet time-to-market objectives. Hierarchy and advanced window management allows multiple views of the same cell, providing the capability to edit in both views. And with Pyxis Layout, engineers can create matched analog layouts quickly by editing using a half-cell methodology.

The dynamic alignment and “move as close as possible” features in Pyxis Layout enable design engineers to manipulate layouts from coarse grid resolutions or large layout views, reducing the number of steps in the layout process and increasing productivity.

**PYXIS IMPLEMENT**

Schematic-driven layout (SDL) is a design methodology that enables design engineers to create “correct by construction” layouts. These layouts are based on information from a schematic or a netlist source.

By using the design connectivity, Pyxis Implement enables the automated creation of layout data, while maintaining the relationship between layout and schematic, reducing design cycle time and ensuring layout is free of LVS violations. Any mix of polygons, device generators (either custom, built-in or from a foundry supplied Process Design Kit), and cell data are supported in the layout environment. Pyxis Implement bridges the gap between schedule and performance goals, offering productivity increases as much as 50X over traditional manual layout methods. Pyxis Implement includes all of the functionality of Pyxis Layout, along with a hierarchical, SDL environment, enabling design engineers to quickly create complex designs without sacrificing layout quality.

Using SDL, design engineers can “pick and place” devices either automatically or graphically. The dynamic connectivity display with cross-probing makes navigation between the layout and schematic fast and easy. The placed devices can then be quickly connected using the built-in interactive router or the optional constraint-driven Pyxis Customer Router.

The engineering change order (ECO) component of Pyxis Implement quickly modifies the layout to reflect schematic-driven engineering changes throughout the design cycle. After comparing the layout with the schematic source, ECO automatically implements design changes in the layout and provides an option to correct the additions, deletions, and property changes, reducing the time required for layout revisions and keeping both the schematic and layout design representations synchronized.

Using the short-checking functionality in Pyxis Implement, design engineers can find potential shorts caused by overlapping nets before running LVS. Design engineers can view the shorts in a browsing menu and make any necessary changes.

Connectivity enables the representation of accurate layout connections at all times in the design cycle. Using connectivity throughout the design process guides designers in creating LVS-correct layout. The compaction feature in Pyxis Implement supports automated area reduction. Semi- or fully automatic compaction allows design engineers to increase productivity without sacrificing layout area. During the design cycle, connections and placements can be created faster at loose constraints; then the layout can be post-processed to achieve tight area constraints.

**AUTOMATED DEVICE GENERATION**

Pyxis Implement supports ready-to-use built-in parameterized device generators for layout design. Whether these device generators are provided in a foundry PDK or created directly by the layout team, they can be used as is or modified to extend the functionality of the device. With Pyxis Implement, engineers can use information stored in the schematic source to automatically create devices that are logically correct and design-rule–compliant, resulting in a dramatic increase...
in productivity over traditional manual method of created the device from its associated layers.

Devices also can be added and modified manually through the use of forms and interactive editing commands. Pyxis Implement speeds the creation of design-rule–correct parameterized devices, resulting in design-rule–correct layouts. Custom devices can also be built, using the base devices as a starting point.

Parameterized layout allows standardization of designs for multiple engineers and remote sites so that DRC correct complex layouts can be created with a simple command, leading to improved productivity.

The transistor device enhances productivity for all designs, including five, six and “n” pin MOS devices that support high-voltage devices and complex memory designs using bent gates. Transistor editing commands offer enhanced flexibility for intricate designs without destroying the device, improving productivity and reliability. The capacitor device creates complex capacitors used in switch capacitors, with a single command, for increased productivity.

The shape-based capacitor device allows design engineers to “fill” areas with capacitors for area savings, and increase flexibility for future design changes. The via device, with multiple subtypes, supports DFM rules as well as “inline” or “turn” routing level transitions in advanced geometry technologies with automatic via selection and rotation. The resistor device supports multiple processes, as well as series and parallel structures. Matched resistors are created with a single command. The guardband device enables design engineers to quickly shield sensitive analog layouts. Guardband editing commands include a cutting ability to complete routing through the guardband to sensitive analog layouts, increasing productivity.

**FLOORPLANNING**

As the complexity of today’s mixed-signal SOC designs continue to grow, planning before layout plays an ever important role. This floorplanning step is supported by Pyxis Assemble, which is completely integrated within the layout environment. Advanced floor planning features include:

- Multiple area estimation modes.
- Layout wire propagation (push/pull through hierarchy with connectivity).
- Hierarchy management.
- ECO flow integration.
- Top-down block boundary editing ability.
- Input from Pyxis Schematic, SPICE netlist, Verilog netlist.
- Read/write LEF/DEF blocks.

**MULTIPLE DESIGNER LAYOUT**

Mentor Graphics developed the optional Pyxis Concurrent environment that enables multiple designer to simultaneously edit the same cell. This is targeted for the final stages of the project, where assemble and DRC/LVS clean-up are being finalized just before tape-out. For more information on this solution, please refer to the Pyxis Concurrent datasheet.

**LAYOUT AUTOMATION**

The interactive routing capabilities of Pyxis Layout Suite include:

- Truly integrated routing technology with pushing for “routing in place.”
- Flexible blockage control.
- On-the-fly visual feedback of length, resistance, capacitance, or costing.
- Intelligent minimization of nets being pushed.
- Multiple bus routing modes.
- Control wire handling for critical nets.

Supported post-routing based DFM improvements in Pyxis Layout Suite include:

- Via minimization.
- Layer swapping.
- Wire bend reduction.

The optional Pyxis Custom Router was developed to meet the routing needs for today’s analog designs. It’s a constraint-driven router that has been qualified at 28 nm. For more information, see the Pyxis Custom Router datasheet.

As the digital content in today’s mixed-signal SOC designs continues to grow, top-level floorplanning and routing becomes an important component in the design
flow. Mentor Graphics developed Pyxis Assemble, which provides a robust set of features for floorplanning, top-level assembly, and interactive routing.

**OTHER CUSTOM METHODOLOGIES**

The Pyxis Layout Suite can be customized to support complex design methodologies. The first of these customizations is for MeMs. One of the unique capabilities included in the Pyxis Layout Suite is the ability for any angle rotation, which is a common operation with MeMs design. The second customization is for the layout of flat panels. An optional product in the Pyxis Layout Suite, Pyxis TFT-LCD, supports same-length and same-layer routing as well as other panel specific design features.

**DESIGN DATA INTERCHANGE**

Pyxis Layout suite supports the interchange of design data through industry standard formats. The supported formats are OpenAccess, LEF/DEF, and GDS.

**LAYOUT VERIFICATION**

Integration with Calibre RealTime provides Calibre signoff-quality physical verification, on-demand, within the Mentor Graphics Pyxis Custom IC Design Platform. Using the same Calibre decks as the signoff flow, design engineers can now verify and optimize their designs while they edit their layouts. With Calibre RealTime, designers can optimize their layouts for performance without sacrificing manufacturing yield.

The Mentor Graphics Custom IC flow and its integrated schematic, extraction, and simulation tools allow you to take a design from system specifications to post-layout verification with a virtually seamless approach.