Benets

• Lowest power with advanced leakage and dynamic power optimization technology
• Highest-quality design with concurrent optimization of power and timing across all corners, modes, and power states
• Lowest clock power with power-aware clock tree synthesis and optimization
• Maximize engineering resources with fully automated low-power flows and UPF support
• Faster power closure with the industry’s highest capacity database, smallest memory footprint and scalable multi-threading

Major Product Features

• Patented MCMM timing and power optimization
• Multi-voltage and Dynamic Voltage and Frequency Scaling (DVFS) flow support
• Industry’s first MCMM CTS for robust, low-power clock trees
• Power grid routing for multiple voltage supplies
• Automatically handles special cells such as level shifters, isolation cells, and MTCMOS switches
• Concurrent multi-Vt optimization, power gating, retention flop synthesis, and power-aware buffering and sizing
• Supports gas station methodology for over-domain routing

The Olympus-SoC low-power platform is the first place-and-route system to offer true concurrent multi-corner, multi-mode closure for both power and timing, giving best quality of results and fast turnaround time for the largest designs at 45 nm and below.

Solving Low-Power Design Challenges

The Olympus-SoC low-power platform comprehensively handles the requirements of low-power design at advanced process nodes. It ensures optimization of the overall solution without excessive iterations, enabling engineers to rapidly deliver fully-optimized, power-efficient designs. Olympus-SoC provides seamless concurrent optimization for both power and timing, covering all process corners, operating modes, and power states through all stages of the flow.

Olympus-SoC completely automates multiple-supply-voltage design flows, including automatic power grid routing for multiple voltage supplies, and support for Dynamic Voltage and Frequency Scaling (DVFS) to handle varying supply voltages and clock frequencies. It automates the placement and routing of special power cells and provides complete graphical analysis, optimization, and verification of power domain cells and connectivity. Olympus-SoC also provides concurrent multi-Vt optimization, power gating, retention flop synthesis, support for gas station methodology, and power-aware buffering and sizing.

To reduce dynamic power, Olympus-SoC provides automatic power-aware clock tree synthesis (CTS) and advanced clock optimization. These capabilities, along with the ability to handle extremely large design data sets, remove unpredictability from the physical implementation process, and improve the cost, performance, and time-to-market of low power ICs.
Concurrent MCMM Optimization

Olympus-SoC delivers concurrent optimization of power, timing, signal integrity, manufacturability, and die size across all design and process corners throughout the design flow. Concurrent multi-corner, multi-mode (MCMM) analysis and optimization is particularly important in multi-voltage design styles, because each different voltage supply and operational mode implies different timing and power constraints on the design. Multi-voltage methodologies cause the number of design corners to increase exponentially with the addition of each domain or voltage island.

Olympus-SoC’s native MCMM kernel seamlessly analyzes and optimizes power across all corners, modes and power states for faster closure of all design requirements.

Flexible Architecture for Multi-Voltage Flows

Along with MCMM timing and power optimization, Olympus-SoC offers an automated multi-voltage design flow, including automatic placement and routing of special cells such as level shifters, isolation cells, and MTCMOS switches.

Olympus-SoC is Unified Power Format (UPF) compliant, so the power intent for multi-voltage that is captured in the UPF file, is carried through the physical design flow. Olympus-SoC can trace connectivity on power pins just like on signal pins, verify the power applied to a given pin, and check isolation cells, level shifters, switches, and retention cells. It automatically creates power domains and the power structures for each supply net, and respects the domain boundaries throughout placement, routing, and optimization.

Power-Aware MCMM Clock Tree Synthesis

Olympus-SoC reduces clock power through a number of advanced synthesis and optimization techniques. To address the large deviations in clock skew across different process corners that occurs at the 65 nm and 45 nm nodes, Olympus-SoC simultaneously optimizes skews across all process corners with MCMM clock tree synthesis and built-in on-chip variation (OCV). Olympus-SoC analyzes flop interactions and derives the exact skew balancing requirements at the different clock tree levels and across different voltage islands. This results in robust, low-power clock trees that are resilient to process variations and show significant improvement in the number of buffers, total area, timing and power. It also simplifies CTS setup because there is no need to manually direct functional skew balancing.

The power-aware CTS includes smart clock gate placement, clock restructuring with cloning and de-cloning, slew shaping, and register clumping to minimize capacitance and reduce power usage in the clocks.

High-Capacity Architecture

Ever-growing design sizes can overwhelm older design tools, but Olympus-SoC’s very high capacity, 100 million+ gates, frees designers to implement their designs flat or hierarchical. The ultra-compact architecture is flexible and open for easy integration into existing design flows.

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