Today's ICs increasingly rely on complex mixed-signal functionality with stringent performance and low power requirements for applications in segments including IoT, Automotive, Communications, and Industrials. Verification of these complex mixed-signal ICs is challenging due to the need to ensure that they meet demanding specifications with correct connectivity, functionality, and adequate system performance across analog/digital (A/D) interfaces on the chip. To address these challenges verification teams need to run an increasing number of mixed-signal simulations at the top level as well as at the sub-system level. These mixed-signal simulation solutions need to be fast, accurate, easy to use, and seamlessly integrate into existing analog and digital verification flows.

Symphony Mixed-Signal Platform is the industry’s fastest and most configurable mixed-signal solution to accurately verify design functionality, connectivity, and performance across A/D interfaces at all levels of the design hierarchy and for all IC applications. Symphony’s modular architecture leverages Mentor’s Analog FastSPICE (AFS) circuit simulator to provide the fastest mixed-signal simulation performance with nanometer (nm) SPICE accuracy and capacity of 20M SPICE elements. With certified accuracy by the world’s leading foundries, AFS delivers 5–10x faster performance than traditional SPICE and 2–6x faster performance than parallel SPICE simulators. Symphony has been proven on a wide range of ICs and IC subsystems including ADCs, transceivers, PMICs, multi-GHz PLLs/DLLs, and sensors.

FEATURES AND BENEFITS

- **Fastest Accurate Mixed-Signal Simulation**
  - Fully leverages AFS advantages
  - Foundry certified nm SPICE accuracy
  - > 5-10x faster than traditional SPICE solvers
  - > 2-6x faster than parallel SPICE solvers

- **Fully Configurable Architecture**
  - Fit-to-Purpose architecture & design-aware technologies
  - Supports industry-leading digital solvers
  - Provides maximum reuse of verification infrastructure
  - Integrated into leading schematic capture flows

- **Best-in-Class Usability**
  - Support for analog/digital-centric flows
  - Ability to reuse A/D command line arguments
  - Powerful A/D boundary element support
  - Save/Restore capability for enhanced productivity

- **Advanced Verification & Debug**
  - Mixed-signal Hi-Z detection
  - Transient noise analysis
  - BE Visualizer with cross-probing for visual context-based debugging
  - Tcl interactive mode for runtime debugging
Symphony's unique, fully configurable design-aware technologies and fit-to-purpose architecture provide verification teams the ability to integrate and optimize their mixed-signal flow for any application. Symphony works with all leading digital solvers, including Mentor's Questa®, allowing users to maximize reuse of their existing verification infrastructure, including testbenches, stimuli, scripts, post processing, encrypted IP blocks, and digital/analog netlists. The digital blocks can be described in Verilog, SystemVerilog, VHDL, or encrypted IP and the analog blocks can be described at the transistor level in industry standard formats or in Verilog-A HDL. Symphony also integrates into the leading schematic capture flows and supports both analog/digital-centric methodologies.

Symphony delivers the industry’s most intuitive use model with a simple configuration file format and command structure. The command line structure allows complete reuse of existing digital/analog solver command line arguments. Symphony offers extensive A/D boundary element (BE) support covering all signal types and multiple power domains including those with dynamic supplies. It is integrated with Mentor's EZwave™ waveform viewer providing a seamless user experience with capabilities such as unified display of A/D waveforms and color coding of waveforms based on design abstraction level.

Symphony’s state of the art debugging capabilities improve efficiency of design error tracing across A/D interfaces. It offers a powerful debugging cockpit called the BE Visualizer to give designers the visual BE context needed to trace back design errors to their sources. Symphony’s interactive Tcl mode allows users to interact dynamically with a running simulation to effectively debug their designs. It leverages interoperability of debug features across the schematic capture tool, waveform viewer, and the simulation kernel to provide a seamless user experience. Symphony’s Save/Restart functionality increases user productivity for specific applications by avoiding simulation reruns.

Symphony offers a powerful set of features designed to increase the verification scope beyond the pure functional realm into verifying performance aspects of the IC. Device noise is critical in nanometer-scale CMOS processes, where it often fundamentally limits circuit performance. Symphony enables gauging the noise impact of analog blocks while preserving the A/D feedback of their parent subsystem which increases the accuracy of the measurement. Symphony leverages AFS’s full-spectrum transient noise analysis capability to accurately predict the device noise impact correlating with 1-2 dB of silicon measurement. Symphony’s Hi-Z checking capability allows users to detect when a mixed-signal net goes into a ‘Z’ state enabling the testbench and the digital control logic to respond correctly to the ‘Z’ state.

Symphony’s best-in-class performance, accuracy, and usability enable a broad range of verification checks including:

- Checking connectivity and functionality at the top level across A/D subsystems
- Ensuring that higher-order analog behavior does not disrupt system functionality due to A/D feedback
- Characterizing analog IP blocks with their digital control included
SYMPHONY MIXED-SIGNAL PLATFORM SPECIFICATIONS

Nanometer SPICE accuracy
> 150 dB transient dynamic range

1K – 20M element capacity

Up to 16 cores with multi-threading support

Transient analysis

Digital HDL support
SystemVerilog
Verilog
VHDL
Real number modeling constructs
Encrypted digital IP

Verilog-A HDL support

Configuration commands
Design configuration
A/D port mapping
A/D boundary element commands

Output formats
Analog: PSF, tr0, nutmeg, FSDB
Digital: FSDB, VCD

Design flow integration
Industry-leading EDA design environment
Command line use model

Built-in A/D Boundary Elements (BE)
Bi-directional
Support for logic, electrical & real types
Multiple power-supply and supply-sensitive BEs
Scoping: net, port, subckt/model, instance

EZwave Viewer support
Unified A/D display with PSF/FSDB
Abstraction based color-coding

Advanced Features
BE Browser
Save/Restart
Transient noise analysis
Hi-Z checking analysis
Auto-detection of power supplies for BEs

Hardware Requirements
Minimum memory recommendation
2 GB of disk space
256 MB of physical memory
512 MB of swap space (virtual memory)

Operating System: Linux®
Redhat®/CentOS 6.5 or higher

For the latest product information, call us or visit: w w w . m e n t o r . c o m