A-XGL2P submodules and data flow.

Ideal for Programmable Logic (FPGA) Implementations

Mentor Graphics® A-XGL2P IP core provides a complete IEEE 802.3ae Ethernet Layer 2 solution when incorporating Mentor’s A-XGMAC and A-XGFIF IP products. The completely integrated solution comprises a Logical Link Control, MAC Control, MAC, and reconciliation sublayer for a 10-Gbps interface between the Network Layer (Layer 3) and Physical Layer (Layer 1) of the Ethernet OSI model. The A-XGL2P offers an IEEE 802.3ae XGMII interface for the link, and an SPI-4 phase 1 compatible interconnect for the fabric interface. There is also a Host interface for register access.

All of the modules in the A-XGL2P IP core have been written specifically to allow implementation in slower technologies, thus allowing easy verification of designs that involve the A-XGL2P in FPGA technologies.

Deliverables:

- Verilog RTL source code
- FPGA-specific constraint and project files
- Verilog functional testbench and associated documentation
- Design documentation

Related products:

- A-XGMAC - 10-Gigabit Ethernet MAC core
- A-XGFIF - 10-Gigabit FIFO core
**Functional Description:**

The A-XGL2P consists of five major blocks: AXGMACP (part of A-XGMAC deliverables); AXGFIFP (part of A-XGFIF deliverables); SPI-4; AXGSTATP; and MXGSAL. (All are depicted in the diagram on the front page.)

The **AXGMACP** 10-Gbps Ethernet MAC module performs packet transmission and reception protocol as described in IEEE 802.3ae. It also includes the MAC control sublayer, as defined in 802.3x.

The **AXGFIFP** 10-Gbps FIFO Interface module provides a data buffering FIFO for communication between the AXGMACP Ethernet interface and the SPI-4 compatible system interface.

**Signal Descriptions:**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTRST</td>
<td>Input</td>
<td>Master Reset</td>
</tr>
<tr>
<td>HSTR</td>
<td>Input</td>
<td>Host Reset</td>
</tr>
<tr>
<td>HOSTC</td>
<td>Input</td>
<td>Host Clock</td>
</tr>
<tr>
<td>HSTSELN</td>
<td>Input</td>
<td>Host Chip Select not</td>
</tr>
<tr>
<td>HSTRWN</td>
<td>Input</td>
<td>Host steady state reset</td>
</tr>
<tr>
<td>HSTRADX</td>
<td>Input</td>
<td>Host read / write port</td>
</tr>
<tr>
<td>HSTDATA[7:0]</td>
<td>Input</td>
<td>Host Register Address</td>
</tr>
<tr>
<td>HSTIDAT[3:0]</td>
<td>Input</td>
<td>Host Input Data</td>
</tr>
<tr>
<td>HSTIDAT[31:0]</td>
<td>Output</td>
<td>Host Output Data</td>
</tr>
<tr>
<td>HSTOE</td>
<td>Output</td>
<td>Host Output Data Enable</td>
</tr>
<tr>
<td>HSTACK</td>
<td>Output</td>
<td>Host Acknowledge</td>
</tr>
<tr>
<td>HSTINT</td>
<td>Output</td>
<td>Host Interrupt</td>
</tr>
<tr>
<td>XGMII[71/35:0]</td>
<td>Input</td>
<td>10-Gbps FIFO Interface module provides</td>
</tr>
<tr>
<td>XGTMIICLK</td>
<td>Output</td>
<td>Fabric Transmit Data Clock, 200MHz Maximum</td>
</tr>
<tr>
<td>TXADD[3:0]</td>
<td>Input</td>
<td>Transmit Address</td>
</tr>
<tr>
<td>TXDATA[63:0]</td>
<td>Input</td>
<td>Transmit Data</td>
</tr>
<tr>
<td>TXEOP</td>
<td>Input</td>
<td>Transmit End of Cell or Packet Indicator</td>
</tr>
<tr>
<td>TXERROR</td>
<td>Input</td>
<td>Transmit Data Error</td>
</tr>
<tr>
<td>TXPTY[3:0]</td>
<td>Input</td>
<td>Transmit Data Parity Indicator</td>
</tr>
<tr>
<td>TXSIZE[2:0]</td>
<td>Input</td>
<td>Transmit Data Size Indicator</td>
</tr>
<tr>
<td>TXSOCP</td>
<td>Input</td>
<td>Transmit Start of Cell or Packet Indicator</td>
</tr>
<tr>
<td>TXVALID</td>
<td>Input</td>
<td>Transmit Data Valid</td>
</tr>
<tr>
<td>TXFULL[3:0]</td>
<td>Output</td>
<td>Transmit Buffer Full Indicators</td>
</tr>
<tr>
<td>RXSTART</td>
<td>Output</td>
<td>Transmit Start Indicator</td>
</tr>
<tr>
<td>RXCLK</td>
<td>Output</td>
<td>MAC Transmit Clock, 156.25MHz</td>
</tr>
<tr>
<td>RXEO</td>
<td>Input</td>
<td>Host Receive Data Clock, 200MHz Maximum</td>
</tr>
<tr>
<td>RXRD</td>
<td>Output</td>
<td>Receive Address</td>
</tr>
<tr>
<td>RXDATA[63:0]</td>
<td>Output</td>
<td>Receive Data</td>
</tr>
<tr>
<td>RXEOP</td>
<td>Output</td>
<td>Receive End of Cell or Packet Indicator</td>
</tr>
<tr>
<td>RXRERROR</td>
<td>Output</td>
<td>Receive Data Error</td>
</tr>
<tr>
<td>RXPTY[3:0]</td>
<td>Output</td>
<td>Receive Data Parity Indicator</td>
</tr>
<tr>
<td>RXSIZE[2:0]</td>
<td>Output</td>
<td>Receive Data Size Indicator</td>
</tr>
<tr>
<td>RXSOCP</td>
<td>Output</td>
<td>Receive Start of Cell or Packet Indicator</td>
</tr>
<tr>
<td>RXVALID</td>
<td>Output</td>
<td>Receive Data Valid</td>
</tr>
<tr>
<td>RXFULL[3:0]</td>
<td>Output</td>
<td>Receive Buffer Full Indicators</td>
</tr>
<tr>
<td>RIXSTART</td>
<td>Input</td>
<td>Receive Start Fill Indicator</td>
</tr>
<tr>
<td>XGMIIM[17:0]</td>
<td>Output</td>
<td>XGMI Transmit Data (156.25MHz, SDR or DDR)</td>
</tr>
<tr>
<td>XGMIIClk</td>
<td>Output</td>
<td>XGMI Receive Data (156.25MHz, SDR or DDR)</td>
</tr>
<tr>
<td>ZGMIIM[17:0]</td>
<td>Input</td>
<td>XGMI Transmit Data and Control Signals</td>
</tr>
<tr>
<td>ZGMIIClk</td>
<td>Input</td>
<td>XGMI Receive Data and Control Signals</td>
</tr>
<tr>
<td>MDIO</td>
<td>Input</td>
<td>MII Serial Data In/Out</td>
</tr>
<tr>
<td>MDC</td>
<td>Output</td>
<td>MII Clock</td>
</tr>
</tbody>
</table>

**Functional Description:**

The SPI-4 (System Physical Interface Level 4) module provides a system-compatible interface for connecting between the Physical Layer (Layer 1) and Link Layer (Layer 3), or between peer-to-peer entities operating at OC-192 rate.

The **AXGSTATP** 10-Gbps Statistics module is a low gate count, register-based statistics module developed for integration with the AXGMACP.

The **MXGSAL** 10-Gbps Station Address Logic module takes the destination address field of incoming packets and all related control signals and performs a hashed address comparison for help in address-based frame filtering.

**Functionality**

The main 802.3ae functionality is provided by the AXGMACP 10-Gbps Ethernet MAC submodule, which is included with the A-XGMAC deliverables. The A-XGL2P has three main interfaces: SPI-4, Host, and XGMII. The SPI-4 compatible interface allows access to the data transmitted and received by the A-XGL2P. The Host interface allows access to the configuration registers of the submodules. The third interface allows access to XGMII-formatted PHY data.

The high-speed data is buffered between the SPI-4 compatible interface and the AXGMACP by separate Transmit (4K) and Receive (8K) FIFOs, which are defined in the AXGFIFP submodule. The A-XGL2P also includes statistics gathering and station address functions. Statistics information is gathered from the data transmitted and received over the Ethernet link by the AXGSTATP submodule, while the MXGSAL submodule provides address filtering and multicast reception capability. The register and data information of both submodules is accessed using the host interface.

**Reference Technology Gate Count:**

**Altera Stratix II Devices:**

- **Total ALUs:** 7657
- **Total Registers:** 6182
- **Total PLLs:** 2
- **Total Memory Bits:** 108,544

**ASIC Gate Count:**

- **Approx. 120,000 gates**

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