Novelics coolROM

The Novelics compiler-based family of advanced embedded memories includes the low-power, high-speed, high-density configurable coolROM™ embedded memory IP, which targets the most demanding applications.

Novelics coolROM embedded memory IP is the industry's highest density ROM. This is achieved with a proprietary bitcell design that requires fewer transistor contacts per cell than conventional designs. A significantly smaller macro size and reduced capacitance results in significant dynamic power dissipation savings.

Novelics coolROM is designed specifically with low-leakage applications in mind. When not in use, the entire ROM core array is automatically maintained with no voltage bias, resulting in zero ROM core leakage. Peripheral circuits utilize positive channel length bias to further reduce leakage.

A high performance cycle frequency is obtained with advanced decoding and sensing circuits.

Creating Custom Memories with MemQuest

The MemQuest memory compiler is a cloud-based on-line tool suite that enables SoC designers to quickly specify and implement custom memories.

FEATURES:

■ High Density
  - Proprietary HD ROM bitcell

■ Low Power Design Support
  - Zero-bias ROM bitcell
  - Transparent light sleep to reduce standby current (source biasing)
  - Multi-VT options (SVT, HVT, uHVT)

■ Flexibility
  - MemQuest memory compiler for PPA optimization
  - Metal-programmable, proprietary HD low-power ROM bitcell
  - Easily configurable options
  - Full porosity above metal 4
  - Fully compatible with Tesson DFT (BIST/BISR and ATPG)
  - Supported in large portfolio of processes and target foundries
  - Custom corner characterization

■ High Yield
  - Silicon-proven architecture in production
  - High-sigma Monte Carlo analysis for reliable operation and performance well beyond normal PVT variation
  - ECC (optional)
  - Advanced manufacturing defect detection through margin setting test modes
  - Fully verified with Calibre® verification platform

■ High Speed
  - Optimized decode circuits
  - Multi-VT options (LVT, uLVT)
  - Bulk-biasing
Customer memory specifications

The custom memory creation process begins by entering the specification for the memory needed in the design. All of the specification parameters that may drive the implementation of a memory are entered into MemQuest in pull-down menu form.

Architecture trade-off analysis

As each memory is specified, a variety of instance solutions are displayed. Each axis of performance is represented with a column in the MemQuest output table. Using this table, the architecture is evaluated and design options are compared and selected based on the requirements for the instance (e.g., area, power, access time, leakage current) and various PVT operating conditions. Many variables — such as wider combinations of muxing and banking — can be expanded. Using the MemQuest flow, instances can be optimized to align exactly with their required characteristics in the chip.

Memory implementation

Once the specification is completed and the architectural tradeoffs chosen, MemQuest immediately generates all of the views and models needed to instantiate the memory in the chip for simulation. Additionally, the design is submitted to the MemQuest cloud servers for physical implementation. A completely automated flow generates the physical implementation of the memory.

Memory verification

Following the generation of the GDSII for the memory instance, a fully automated verification flow will be run on each instance. Verification includes RC extraction, SPICE simulation, timing model checks, and physical verification. Individually characterized and verified instances will be released on a cloud server for customers to download.

MemQuest Deliverables

- Product Manual
- Datasheet
- Verilog RTL Model
- Liberty Model
- LEF
- ROM Programming Script
- Tessent MBIST Model
- Tessent ATPG Model
- LVS Netlist
- GDSII

For the latest product information, call us or visit: www.mentor.com

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