- Binary and Memory cycle compatible with Intel 8051 Designs
- Fast 2-clocks per machine cycle implementation
- Richly-featured hardware debugger: multiple breakpoints, instruction traceback, single step execution. Full debug access to all registers and memory spaces
- 1Mbyte program and data address spaces
- Memory interfaces may be configured for synchronous or asynchronous devices
- External interfaces support wait states
- Optional demultiplexed program and data interfaces
- Optional single machine cycle memory accesses
- Up to 8 16-bit data pointers
- 25-input, five level interrupt controller
- Full implementation of legacy peripherals: 32 GPIO ports, 3 16-bit counter timers and a full-duplex serial port. All legacy peripherals are optional
- Watchdog timer
- 2-wire and 4-wire interfaces
- Pulse width modulator array
- Flexible interfacing options for external peripherals
- Power saving modes: powerdown, stasis, idle and run

M8051EW Architecture
Overview
The M8051EW is a highly configurable soft-core implementation of the industry standard 8051 microcontroller that features a two-clocks-per-machine cycle architecture. Use of standard synchronous design methodology makes this core simple to integrate into both ASIC and FPGA SoC designs.

Configurable
The core RTL is highly configurable at compile time. Major configuration options include:

- Combined program and data address space or Harvard architecture
- Optional 20-bit (1Mbyte) extended memory addressing scheme with additional stack
- Number of 16-bit data pointers (1, 2, 4 or 8)
- Each memory component may use a synchronous or asynchronous interface
- Hardware multiplier/divider is optional
- The number of interrupt sources (up to 25) and priority levels (up to 5)
- All peripherals are optional and may be excluded if not required
- Debug traceback depth and number of hardware triggers selectable

Configurable Peripherals
The core RTL includes the following peripherals as standard:

- Three timer/counters
- Legacy UART
- Watchdog timer
- 2-wire interface
- 4-wire interface
- Pulse width modulator array, with ramping option

All the non-legacy peripherals include a configurable clock prescaler, and have configurable base addresses and interrupt channels.

Power Management
The M8051EW offers three power saving states. These are implemented by dividing the core logic into several synchronous clock domains using optional clock gates. These reduce power consumption by 75% in the idle state and to leakage levels in the stasis and powerdown states. The microcontroller can be awoken from idle and stasis states using interrupts.

Programming Support
The core runs all standard 8051 binary code. Syntill8 recommends Keil C51 and IAR Systems compilers for code development. These compilers can optimise code by making use of the M8051EW data pointer and interrupt extensions.

Debug Support
The M8051EW includes comprehensive on-chip instrumentation accessed by external debug environments via a 4-wire JTAG port. Debug features include start/stop/step/hardwire and software breakpoints, execution traceback, and full read/write access to all memory and SFR locations. The M8051EW debug interface is designed to be compatible with FS2 System Navigator debug system.

Deliverables
- VHDL '93 and Verilog 2001 RTL source code
- RTL configuration script
- VHDL and Verilog Testbenches
- Demonstration assembly code
- Simulation scripts for Modelsim and Cadence
- Synopsys synthesis compile scripts and SDC timing constraint files.
- Example Mentor DFT and ATPG scripts
- Example netlist implementation with SDF files
- Detailed product specification and a user guide containing implementation notes.

M8051 Product Selector

<table>
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<tr>
<th>Design</th>
<th>Clocks per Machine Cycle</th>
<th>External Address Space</th>
<th>Internal Data Memory</th>
<th>Multiplexed External Bus</th>
<th>Wait States</th>
<th>Synchronous Support</th>
<th>Internal Sources</th>
<th>Nondisableable Interrupts</th>
<th>Interrupt Levels</th>
<th>Data Pointers</th>
<th>I/O Ports</th>
<th>Timer Counters</th>
<th>Serial Port</th>
<th>Memory Banking</th>
<th>External SFR Wraparound</th>
<th>On-chip Debug</th>
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M8051EW Datasheet
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