Overview

The MUSBHSFC OPB core provides a USB function controller that conforms to the USB 2.0 specification for High/Full-speed (480/12 Mbps) functions.

The core is user-configurable for up to 15 IN endpoints and up to 15 OUT endpoints in addition to Endpoint 0. These additional endpoints can be individually programmed for Bulk/Interrupt or Isochronous transfers.

Each endpoint requires a FIFO to be associated with it. The MUSBHSFC has a RAM interface for connecting to a single block of synchronous single-port RAM (added by the user.) The FIFO for Endpoint 0 is fixed at 64 bytes. The other endpoint FIFOs may be from 8 to 8192 bytes in size and can buffer either 1 or 2 packets. Separate FIFOs may be associated with each endpoint: alternatively an IN and an OUT endpoint with the same Endpoint number can be configured to use the same FIFO, for example to reduce the size of RAM block needed.

The MUSBHSFC OPB provides a USB 2.0 Transceiver Macrocell Interface to connect to an 8-bit High/Full-speed transceiver. Access to the FIFOs and internal control/status registers may be via a 16/32-bit BVCI*-compatible synchronous CPU interface or via the OPB bridge.

The MUSBHSFC OPB has a RAM interface for connecting to the single block of synchronous RAM that is used for all the endpoint FIFOs. The device also offers support for DMA access to the endpoint FIFOs. (The optional MUSBHSFC – AHB bridge includes a built-in DMA controller.)

The MUSBHSFC OPB provides all the USB packet encoding, decoding and checking – interrupting the CPU only when endpoint data has been successfully transferred. A graphical user interface script is provided for configuring the core to the user’s requirements. (Note: Configuration GUI developed and tested using Tcl/Tk 8.3. Use with an earlier version of Tcl/Tk may give unpredictable results.)

Major Product Features:

- Complies with USB 2.0 standard for High/Full-speed (480/12 Mbps) functions
- Configurable for up to 15 additional IN or OUT endpoints
- Configurable FIFO sizes from 8 to 8192 bytes, with option of dynamic FIFO sizing
- Standard Device Requests handled efficiently in software for flexibility
- UTMI Transceiver Macrocell Interface
- OPB Interface wrapper 32-bit
- Support for DMA access to FIFOs
- Synchronous RAM interface for FIFOs
- Supports Suspend and Resume signaling
- Soft connect/disconnect option
- Fully synthesizable
- Scan test ready
- Graphical User Interface provided for core configuration

Deliverables:

- Verilog source code
- Synthesis script for Design Compiler
- Verilog testbench
- Sample firmware
- Product Specification; User Guide; Programmer’s Guide

Related Products

- MUSBFSFC USB 1.1 Full-Speed Function Controller
- MUSBFDRC USB On-The-Go Full-Speed Dual Role Controller

* Basic Virtual Component Interface, as defined by VSIA (OCB 2 v1.0)
Inventra™ MUSBHSFC OPB USB 2.0 High-Speed Function Controller

Structure
The MUSBHSFC OPB function controller consists of a UTM re-synchronizing block, a Packet Encoder/Decoder plus CRC Generator/Checker block, RAM Controller, MCU Interface, plus a control block for each endpoint.

The function controller interfaces to a UTM specification v1.05 USB 2.0 transceiver macrocell.

UTM Sync Block
The role of this block is to resynchronize between the transceiver macrocell 30/60 MHz clock domain and the function controller’s user-supplied clock (>30 MHz). This allows the rest of the MUSBHSFC OPB to run from the bus clock without requiring any further synchronization. The 8-bit transceiver interface is converted to 16-bits so that a user clock down to 30 MHz can be used. The block also performs the high-speed detection handshaking.

MCU Interface
The core may be interfaced to a range of different CPU bus standards. The interface provided by the MUSBHSFC itself is a 16/32-bit synchronous CPU interface that is compatible with the VSIA standard ‘BVCI’ Basic Virtual Component Interface. Connection to other standard buses may be provided through the addition of optional bridges such as the MUSBHSFC – OPB bridge which is provided with the core.

Packet Encoder/Decoder
The Packet Encoder/Decoder block generates headers for packets to be transmitted and decodes the headers of received packets. It also performs CRC generation and checking.

Endpoint Controllers
Two controller state machines are used. One for control transfers over Endpoint 0, and one for bulk/interrupt/isochronous transactions over Endpoints 1 to 15.

RAM Controller
The RAM Controller provides an interface to a single block of synchronous RAM, which is used to buffer packets between the MCU and the USB.

It takes the FIFO pointers from the endpoint controllers, converts them to address pointers within the RAM block and generates the RAM access control signals.

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<table>
<thead>
<tr>
<th>Signal Interface Signals</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCLK</td>
<td>Input</td>
</tr>
<tr>
<td>XCVRSEL</td>
<td>Output</td>
</tr>
<tr>
<td>TERMSEL</td>
<td>Output</td>
</tr>
<tr>
<td>SUSPENDM</td>
<td>Output</td>
</tr>
<tr>
<td>LINESTATE[1:0]</td>
<td>Input</td>
</tr>
<tr>
<td>OPMODE[1:0]</td>
<td>Input</td>
</tr>
<tr>
<td>XDATAOUT[16:0]</td>
<td>Input</td>
</tr>
<tr>
<td>RXVALID</td>
<td>Input</td>
</tr>
<tr>
<td>RXVALIDH</td>
<td>Input</td>
</tr>
<tr>
<td>TXREADY</td>
<td>Input</td>
</tr>
<tr>
<td>XDATAIN[16:0]</td>
<td>Input</td>
</tr>
<tr>
<td>RXERROR</td>
<td>Input</td>
</tr>
<tr>
<td>XERRINT</td>
<td>Input</td>
</tr>
</tbody>
</table>

Configuration Options
The MUSBHSFC OPB is user-configurable for:
1. The number of endpoints that support IN/OUT transfers.
2. FIFO sizes: Ep0 64 bytes; Eps 1 to 15: 8 to 8192 bytes.
3. Whether any IN/OUT FIFOs are shared

Reference Technology Gate Count: 11000 + 1700/1800 for each additional endpoint (or 2700/2800 per endpoint if dynamic FIFO sizing required); + 2200 for High-Bandwidth support; + 2400.