Automotive-grade ATPG
Tessent TestKompress

Test Methodology for Zero-defect IC Test

Tessent® TestKompress® with Automotive-grade ATPG overcomes the quality limitations of traditional DFT methodologies by targeting defects in ICs at the transistor and interconnect levels. The Automotive-grade fault models and test patterns capture defects that go undetected with traditional methodologies. Capturing these otherwise undetectable defects helps the makers of digital ICs meet the ISO 26262 goal of zero defective parts per billion (DPPB).

Tessent TestKompress with Automotive-grade ATPG contains a suite of fault models and test pattern generation applications that can be used separately or together. It is the result of decades of research in cell-aware, layout-aware, and defect-oriented test and modeling. These technologies were developed in collaboration with foundries, fabless companies, and integrated device manufacturers (IDMs). Tessent TestKompress with Automotive-grade ATPG has been validated on millions of tested devices representing mature planar process nodes, as well as state-of-the-art FinFET processes.

With Tessent TestKompress Automotive-grade ATPG, users can reach DPPM levels that would otherwise only be possible by combining ATPG patterns with extremely expensive functional or system-level tests.

Cell-aware Test

Mentor’s CellModelGen fault model extraction makes TestKompress cell-aware stand out from the crowd. The CellModelGen fault extraction uses layout-annotated Spice representation of the cells to identify the location of possible transistor, bridge, open, and port defects. The cell layout is analyzed for potential bridge defects by calculating the critical area of each potential defect and its related defect probability. This analysis generates a model that ensures

FEATURES:
- Transistor-level ATPG (cell-aware) based on cell layout to target defects internal to library cells.
- Critical-area based bridge and open ATPG to target the most significant interconnect defects.
- Cell-neighborhood (inter-cell) ATPG to detect bridge defects between cells.
- Static, delay, and timing-aware test.
- Targets defects in both combinational and sequential cell types.
- Fully compatible with all Tessent Hierarchical ATPG, Embedded Deterministic Test (EDT), and VersaPoint™ test points for minimizing test cost.
- Combine with Tessent Diagnosis cell-aware and layout-aware diagnosis for a complete end-to-end defect detection and diagnosis solution.
- Leverages same LEF/DEF-based layout database (LDB) used by Tessent Diagnosis.

BENEFITS:
- Enables significant improvements in product quality levels without large increases in test costs.
- Address new defect mechanisms in leading edge technology nodes.
- All Tessent products are part of the Mentor Safe program and qualified for all ASIL ISO 26262 projects with a complete set of certified ISO 26262 documentation.
- Mentor Graphics award-winning customer support and consulting services ensure success.
the highest possible defect detection, minimizes pattern count, and preserves required information for diagnosis. Reporting mechanisms enable the analysis of the potential improvement in defect coverage at the cell level. Layout marker files are produced to aid in debug and diagnosis.

Critical Area-based Interconnect Test
To keep ATPG manageable, bridging faults must be extracted from the layout to obtain nodes that are physically close together. Rather than relying on complex flows with DRC/LVS tools, Tessent TestKompress with Automotive-grade ATPG uses the same layout database (LDB) that is used by Tessent Diagnosis layout-aware diagnosis. The extraction process automatically ranks bridges and opens on critical area, allowing ATPG to focus on the most important defect locations.

Cell-neighborhood Test
Some bridge defects cannot be targeted by cell-aware or interconnect bridge extraction. To target bridge defects between standard cells, the layout of the design and of the standard cells must be considered. Tessent analyzes the design to identify cell-neighborhood combinations, taking rotations, flips, and offsets into account, based on the layout database (LDB). This information is used by the CellModelGen tool to create the fault model definitions for the most important neighbor combinations.

Test Pattern Generation Flow
Cell-aware ATPG requires a per-library characterization. Interconnect defects are extracted once per design from the design layout. From that point forward, the test pattern generation is identical to that of traditional fault models.

Product Requirements
Cell-aware fault model files may be available from your library provider. Cell-aware model generation is also offered as a service by Mentor Consulting. Users can also generate their own models. This will require Mentor’s CellModelGen-Plus or Eldo, as well as a layout extraction tool such as Calibre xRC/xACT. Interconnect and cell-neighborhood ATPG requires a Tessent layout database (LDB) created from LEF/DEF.

Tessent DFT and Yield Analysis
Tessent TestKompress with Automotive-grade ATPG is part of Mentor’s industry- and technology-leading product family for IC test and yield analysis. The Tessent products include integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on Linux.

Tessent TestKompress with Automotive-grade ATPG test pattern generation flow.

For the latest product information, call us or visit: w w w. m e n t o r. c o m/ t e s s e n t

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