Need a Silicon Test Solution with Built-In Flexibility?

The Tessent® product family is a comprehensive silicon test and yield analysis solution that addresses the challenges of manufacturing test, debug, and yield ramp for today’s SoCs. Built on the foundation of the best-in-class solutions for each test discipline, Tessent brings them together in a powerful test flow that ensures total chip coverage.

The flexibility of the Tessent product family enables high-quality tests to be applied throughout the product life cycle—from wafer and package test to burn-in, in-system, and field test. Accurate yield analysis is achieved by exploiting the structural nature of scan test and BIST methodologies and correlating to physical features.

The full Tessent product family combines deterministic scan testing, embedded pattern compression, built-in self-test, specialized embedded memory test and repair, boundary scan, mixed-signal test, and silicon learning technologies.

Contact Tessent@mentor.com

www.mentor.com/tessent
Mentor Graphics provides comprehensive solutions for yield analysis, diagnosis, debug, and characterization of digital semiconductor devices:

**Tessent Diagnosis** identifies defects causing ATPG pattern failures. Layout-aware and cell-aware diagnosis technology ensures the most precise results for interconnect, cell-internal, and scan chain defects. Diagnosis requires test patterns from Tessent TestKompress or Tessent FastScan.

**Tessent YieldInsight** is specialized for understanding and identifying yield loss from scan test data and making volume diagnosis results actionable. It removes ambiguous results from diagnosis and identifies underlying root causes and systematic yield limiters.

**Tessent SiliconInsight** provides an automated interactive environment for test bring-up, debug, and silicon characterization of devices tested with Tessent TestKompress, FastScan, MemoryBIST, LogicBIST, or containing IJTAG instruments inserted with Tessent IJTAG. ATE data collection and diagnosis of BIST-tested memories and logic is also supported.

**Diagnosis-Driven Yield Analysis**

Tessent YieldInsight provides advanced statistical analysis and data mining facilities that complement the automated diagnosis capabilities in Tessent Diagnosis. This solution enables IC manufacturers to identify the probable cause of systematic defects before physical failure analysis. YieldInsight significantly reduces the time it takes to identify the root cause of yield loss and finds yield limiters that may otherwise go undetected.

**Silicon Debug and Characterization**

Tessent SiliconInsight reduces silicon bring-up time for devices tested with Tessent DFT structures and/or ATPG patterns. The software enables an interactive bench-top environment for experimentation, debug, and characterization. Up to 120 device pins can be accessed using a USB-to-digital adaptor and your existing debug or validation board.

Visit our website at www.mentor.com/tessent