Industry Leading ATPG Solution

Advanced design techniques used in today’s SoCs present significant challenges to achieving high-quality silicon test. Tessent® FastScan™ is the gold standard in automatic test pattern generation (ATPG), with support for a wide range of fault models, comprehensive design rule checks, extensive clocking support, and innovative algorithms for performance-oriented pattern compaction. Its ability to be applied to any type of design makes it the most versatile ATPG solution available. Tessent FastScan is part of the Tessent Shell platform, which offers extensive capabilities for automation, customization, testability analysis, and debug.

High Test Quality

Tessent FastScan supports all traditional fault models used for uncovering both static and dynamically activated defects. Timing-aware test uses SDF to ensure that the long paths in the design are tested. Bridge defects can be addressed using embedded multi detect or deterministically based on the design. Support for user-defined fault models (UDFM) also allows virtually any defect mechanism to be modeled and targeted. While traditional fault models only consider faults on cell inputs and outputs and on interconnect lines between these, Tessent FastScan’s cell-aware test targets defects inside the standard cells. Cell-aware test leverages a unique fault model that is created using a process that extracts shorts, opens, and transistor defects based on the Spice model of the cell.

High test quality is more than just fault models, it is also about minimizing the impact of unknown states in the design. False and multi-cycle paths are analyzed effectively to minimize the impact on test coverage.
**Flexibility**

Tessent FastScan supports any design flow and any common structured scan architecture. Unlike other tools that require a specific set of homogenous EDA tools for operation, Tessent FastScan is designed to work in all design environments using any combination of synthesis, place-and-route, and verification tools. When the scan structures are created using Tessent Scan or Tessent ScanPro, setup information for Tessent FastScan is automatically generated. Tessent FastScan also recognizes scan setup information from other scan insertion tools in industry standard IEEE 1450 STIL format.

To ensure reliable at-speed test, Tessent FastScan supports on-chip PLLs and OCC, whether inserted by Tessent ScanPro or other tools.

**Test Pattern Compaction**

Tessent FastScan is known for delivering high-coverage, compact test sets. The integrated ATPG Expert automatically optimizes coverage and pattern count with shortest run time. It monitors progress, learns, and adjusts during your ATPG run.

With the growing need to improve test quality with at-speed and cell-aware patterns, the amount of test data can still be an issue. In these situations, Tessent TestKompress® with embedded deterministic test (EDT) technology can be used to provide the most compact pattern set. Both tools use the same efficient engine.

![Tessent FastScan can leverage on-chip PLL and on-chip clock control for reliable at-speed test.](image)

**Productivity**

Tessent FastScan is built on the Tessent Shell platform, which offers powerful TCL-based scripting, automation, and introspection.

The Tessent DFTVisualizer™ viewing environment is integrated within Tessent FastScan for viewing and correcting testability problems. Tessent DFTVisualizer shows the design in various views such as schematic, design structure, waveform, library, data, hierarchy, and additional views to facilitate viewing and troubleshooting. Common debugging tasks, such as DRC analysis simulation mismatch debugging are automated.

Tessent DFTVisualizer’s ATPG statistics reporting provides detailed analysis of untestable faults and classifies them into easy-to-recognize categories that simplify the debugging of low test coverage issues.

![T Tessent TestKompress is recommended when test data increases due to gate count and test quality requirements.](image)

**Tessent DFT and Yield Analysis**

Tessent FastScan is part of Mentor’s industry- and technology-leading tool suite for IC test and yield analysis. The Tessent product family includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on Linux.

For the latest product information, call us or visit: [www.mentor.com/Tessent](http://www.mentor.com/Tessent)

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