Automation of the IEEE 1687 Standard
Tessent IJTAG

Designing a modern product requires the integration of multiple IP blocks from both in-house and third party sources. The Mentor Graphics Tessent® IJTAG solution delivers comprehensive automation support for implementing the IEEE 1687 standard, providing plug-and-play IP test and instrumentation integration. Tessent IJTAG can be used by IP providers to ensure compliance to the standard as well as by chip designers to efficiently integrate IEEE 1687 compliant IP from various sources into their designs. These capabilities are critical to support the growing amount of IP used in today’s large SoCs.

IEEE 1687 Standard Overview
The IEEE 1687 standard creates an environment for plug-and-play integration and use of the instrumentation portions of IP blocks. Instrumentation includes test, debug, and monitoring functions within the IP. The standard defines hardware rules related to the instrumentation interfaces and connectivity between these interfaces, a language to describe these interfaces and connectivity (Instrument Connectivity Language, or ICL), and a language to define operations to be applied to individual IP blocks (Procedural Description Language, or PDL).

IEEE 1687 Certification for IP
Supporting the IEEE 1687 standard provides several benefits to IP providers. It makes their products easier to integrate and hence more attractive to a wider customer base. It also provides improved testing and debugging capabilities and an overall more robust product. Tessent IJTAG lets IP providers verify that their IP is compliant to the IEEE 1687 standard. IP developers must create ICL that describes the IP in isolation, and PDL routines that describe usage of the IP.

Tessent IJTAG can be used to create simulation testbenches that verify the ICL against the IP’s Verilog description. It can also convert PDL routines into Verilog.
for verification against the IP’s ICL description using automatically generated simulation testbenches.

**IP Integration and Usage**

For the designer, IEEE 1687 enables robust integration and validation of various IP blocks into a larger design. It also provides several other benefits including activation of BIST (Built-In Self-Test) functionality and the observation of the test results, retargeting of IP-level control and access patterns to the top level of the chip, and on-the-fly test plan modification, with serial or parallel test execution of different IPs as needed.

Successful application of the standard requires comprehensive automation support. Tessent IJTAG delivers this necessary automation through a number of key capabilities.

**ICL Extraction and Verification**

Tessent IJTAG provides automatic extraction into ICL of interconnections between IJTAG-compliant IP blocks within an IEEE 1687 network. The user only needs to provide ICL for the leaf IP blocks. Extraction can be performed at any level of the hierarchy to enable early verification. Support includes simulated setup to place the block or chip being extracted in ‘1687 mode.’ The extracted ICL descriptions are also verified against an integrated set of Design Rule Checks.

**IEEE 1687 Network Insertion**

Tessent IJTAG provides a flexible IEEE 1687 network creation and insertion flow that supports any IEEE 1687 compliant IP. The flow supports automatic insertion based on a user-specified network definition. Pre-inserted IEEE 1687 compliant IP blocks are automatically detected and handled as part of a multi-pass insertion capability. Powerful design editing and introspection commands are also supported for customization. Editing can be performed at the RTL or gate-level. Introspection commands provide access to IEEE 1687 information such as attributes and parameters.

**PDL Command Retargeting**

Retargeting consists of translating PDL commands written for an IP block in isolation to new PDL commands that can be applied at a chosen level within the IEEE 1687 network hierarchy. Tessent IJTAG supports both retargeting as well as merging of PDL commands for multiple IP blocks. The highly efficient merging process results in minimum cycle counts for IP access within a reconfigurable IEEE 1687 network. Commands retargeted to chip pins can be translated to common ATE pattern formats or to Verilog for simulation. Chip-level PDL patterns are also supported by Tessent SiliconInsight® for interactive debug.

**Tessent Silicon Test and Yield Analysis Solutions**

Tessent IJTAG is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on Linux.

For the latest product information, call us or visit: [www.mentor.com/silicon-yield](http://www.mentor.com/silicon-yield)