Embedded Memory Self-Test, Repair, and Debug
Tessent MemoryBIST

Hierarchical Tessent MemoryBIST infrastructure.

Industry-Leading Solution for Memory Built-In Self-Test
Mentor Graphics’ Tessent® MemoryBIST provides a complete solution for at-speed testing, diagnosis, repair, debug, and characterization of embedded memories. The solution’s architecture is hierarchical, allowing BIST and self-repair capabilities to be added to individual cores as well as at the top level.

On-chip generated test patterns are delivered to the memories at application clock frequencies. The Tessent MemoryBIST controllers are configurable to support a variety of memory types, as well as a range of memory timing interfaces and memory port configurations. The controllers are accessed and controlled through an IEEE 1687 (IJJTAG) network. This highly configurable network is used to access all Tessent IP and can support any 3rd party IJJTAG-compliant instruments. The controllers can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug, and in-system test.

Tessent MemoryBIST includes a comprehensive yet flexible implementation flow built on the Tessent Shell platform. Full access to design and pattern data and extensive design editing capabilities enable powerful design-independent flow scripting. Automation is provided for design rule checking, test planning, BIST integration, and verification all at the RTL or gate level. The back-end flow for memory test (debug and characterization) is managed by Tessent SiliconInsight®, an interactive, desktop-based debug environment.

Hard Algorithm Programmability
At design time, one or more Mentor-provided or user-developed memory test algorithms can be hard-coded into a Tessent MemoryBIST controller. Any of these algorithms can then be applied to each memory through run-time control. This capability is useful for optimizing test time by selecting shorter test algorithms as the manufacturing process matures. The hard programming feature includes the following capabilities:

• Flexible BIST IP integration automation shortens time-to-market.
• Design-time algorithm specification allows for quality improvement and test time optimization.
• Field algorithm specification provides full control of quality and test time trade-offs.
• Built-in row- and column-based repair analysis reduces test time for repairable memories.
• Single insertion memory repair on any tester reduces manufacturing costs.
• Desktop-based test debug and characterization speeds time-to-market.

FEATURES:
• Design-time algorithm specification supports hardcoding of custom test algorithms. Innovative architecture supports the programming of any test algorithm.
• Field algorithm specification supports run-time downloading of test algorithms. Full automation provided for downloading program code through the TAP or CPU interface.
• On-chip global eFuse management includes fuse data compression and programming.
• On-chip test and repair supports third-party repairable SRAMs.
• Self-repair supports any number of power domains distributed across any number of physical blocks.
• Supports any level of parallelism for both test and repair activities.

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• High-level programming language for straightforward algorithm specification.
• Access to a large library of common memory test algorithms.
• Library of algorithm program code is included for direct use or as a reference for creating modified algorithms.

**Field Programmable Option**
The Tessent MemoryBIST Field Programmable option allows any memory BIST controller to include full run-time programmability. With this feature implemented, any user-programmed memory test algorithm can be downloaded into the BIST controller while on the tester or in-system. This capability allows any unforeseen defect mechanism to be dealt with without a design re-spin. Both the hard and soft programming features can be used within the same BIST controller.

**Power-Aware Self-Repair Option**
The Tessent MemoryBIST repair option eliminates the complexities and costs associated with external repair flows. It tests and permanently repairs all defective memories in a chip using virtually no external resources. The Tessent MemoryBIST self-repair architecture uses programmable fuses (eFuses) to store memory repair info. During memory test, built-in repair analysis engines within each BIST controller calculate the fuse information needed to repair each memory. Fuse information can be accumulated over different test conditions. The final data is stored in a local self-repair (BISR) register that is part of a single serial chain specific to a power domain. These serial chains are then used by a fuse controller to shift and compress repair data into a central eFuse array. Hard incremental repair is also supported, allowing the results of additional repair analysis performed during subsequent manufacturing test steps or in-system to be added to the stored fuse information.

Whenever a power domain is powered-up, the fuse controller transfers relevant fuse information from the eFuse array to each memory in the domain. Tessent MemoryBIST supports two transfer mechanisms. The same single serial chain can be used to minimize routing overhead, or a parallel broadcast approach can be used to minimize repair time. In the latter case, multiple eFuse arrays distributed across cores can be used to minimize routing.

**Shared-Bus Interface Support**
Processor cores from vendors such as ARM can provide a shared-bus interface to the memories internal to the processor core IP. This interface provides a standard set of test address, data, and control ports to access all memories embedded within each processor core. The memory BIST controller no longer communicates directly to each memory but must now understand how to gain access to each memory through the common interface signals and, in addition, must...
account for the different levels of pipelining to and from each memory.

Tessent MemoryBIST supports integrating memory BIST and repair capabilities into a design that contains both stand-alone memories and memories embedded within an IP core that are only accessible through a shared-bus interface.

External Memory and 3D-IC Support
Tessent MemoryBIST provides support for testing memories that are external to the device containing the BIST IP. Support is provided for both stand-alone memory packages at the board-level and for the rapidly growing use of 3D packages consisting of one or more memory die stacked on top of a separate logic die.

Testing 3D stacked memory die.

The memory BIST control logic is integrated into the logic chip allowing at-speed testing of the memory bus logic and connections. Both bond wire and through-silicon via (TSV)–based interconnects can be tested. The Shared-Bus interface support also enables testing package configurations in which multiple memory die are stacked and connected to a single logic die via the same electrical interconnects. The field programmability supports changes in the memory die, or variant stacks that use different memory designs.

Test Debug and Characterization
Tessent SiliconInsight provides a desktop-based interactive debug and characterization system. Designers can execute tests, collect data, and generate shmoo plots for any selection and order of BIST-tested blocks on the device. Tessent SiliconInsight can greatly increase productivity during silicon validation and debug, speeding time-to-market.

Tessent Silicon Test and Yield Analysis Solutions
Tessent MemoryBIST is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on Linux. For more information, visit www.mentor.com/silicon-yield.