Tessent SerdesTest
Parametric Embedded Test for SerDes Transceivers

Industry Leading Solution for Embedded Testing of SerDes IO
Mentor Graphics Tessent® SerdesTest provides complete, parametric, embedded test for multi-Gb/s SerDes. The solution measures waveshape, many types of jitter, and various jitter tolerance parameters, all in less than 200 ms, including test set-up and on-chip comparison to test limits via an IEEE 1149.1 TAP interface. Tessent SerdesTest uses unlimited time-resolution analysis (ULTRA) patented technology connected to only the SerDes parallel ports, and has been proven on customer silicon operating faster than 10 Gb/s. One 10k-gate ULTRA module can test any number of SerDes lanes, and a TAP (or IEEE 1500 WTAP) can interface to any number of ULTRA modules.

Embedded Undersampling-Based Measurement
ULTRA technology uses undersampling to achieve virtually unlimited, silicon-proven time resolution—from 1 second to 100 femtoseconds—using a purely digital analysis logic block synthesized from RTL in a standard digital design flow. Undersampling, when high frequencies are sampled by lower frequencies, is used by most test equipment, and is often described as “equivalent time sampling,” “mixing down,” or “aliasing.”

Stimulus data for the SerDes-under-test is generated by the Tessent SerdesTest IP as clock-like or pseudorandom data supplied synchronously to the TX parallel input port. Voltage-related tests are performed while injecting an offset DC volt-

Key Benefits
• Shorter test times and minimal tester hardware requirements reduce tests costs.
• Proven picosecond accuracy for any PLL, on any ATE, lowers test cost.
• Characterizing with PC plus GPIB-controlled benchtop equipment or microWire-controlled clock conditioner PLL shortens time-to-market.
• Mentor Graphics award-winning customer support ensures success.

Key Features
• Jitter measurement with sub-picosecond accuracy: Histogram or RMS, HF jitter with golden PLL cut-off, duty cycle distortion, transition-density dependent delay.
• Waveshape measurement: Slew rate or 20–80% transition time and amplitude.
• Jitter tolerance parameters measurement: Mean sampling instant, systematic sampling errors in receiver, jitter in recovered clock.
• Lane performance measurement: Bit errors in all lanes simultaneously, BER in multiple lanes simultaneously.
• Design and test automation: RTL insertion and testbench generation, characterization and production tests, repeatability analysis.
Measurement resolution and test time are inversely proportional to the sampling clock’s frequency offset from being synchronous to the PLL’s reference clock frequency, hence are adjustable and require no calibration. The golden PLL cut-off frequency is linearly proportional to this frequency offset.

**Interactive Debug**

Tessent SerdesTest includes the Mentor Graphics Tessent SiliconInsight Mixed-Signal solution. With this interactive capability, any of the supported SerDes embedded tests can be instantly run on a PC or tester. The GUI displays all measurement results in engineering units and automatically compares these results to the limits that were shifted into the chip. This allows for detailed characterization and easy setting of production test limits.

**Supported Embedded Measurements**

- **Waveform**
  - TX logic levels, based on DC measure by ATE’s PMU while transmitting each of two patterns.
  - RX logic levels, based on DC offset injected by ATE’s PMU to obtain <10% or >90% duty cycle.
  - Slew rate and/or transition time.

- **Jitter**
  - RJ, based on jitter histogram for clock-like bit pattern and histogram shape.
  - TJ, based on jitter histogram for pseudorandom bit pattern.
  - DCD, based on duty cycle for 1010 bit pattern.
  - ISI, based on steady-state transition-density dependent delay for two or more densities.

- **Jitter tolerance**
  - ISI for different equalization settings.
  - Mean sampling instant (MSI) in signal eye, and systematic variations for each bit position.
  - Jitter in recovered parallel-rate clock.
  - Bit error rate for standard PRBS7 pattern, in presence of offset or spread spectrum clocking.

**Tessent Silicon Test and Yield Analysis Solutions**

Tessent SerdesTest is part of the Mentor Graphics industry-and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.