Hierarchical ATPG Compression
Tessent TestKompress

Tessent TestKompress uses Embedded Deterministic Test technology to achieve the highest level of test quality while compressing scan patterns often 100X or more.

Industry Leading Scan Test Tool
The TestKompress® industry-leading automatic test pattern generation (ATPG) tool delivers the highest quality scan test with the lowest manufacturing test cost. TestKompress uses a patented on-chip compression technique to create scan pattern sets that have dramatically less test data volume, which reduces test time on the automatic test equipment. Support for advanced fault models includes cell-aware faults to ensure maximum defect coverage. TestKompress supports a hierarchical test approach that is the most effective test approach for today’s large and ever-growing design sizes. TestKompress can also be combined with Tessent LogicBIST to implement a hybrid solution that maximizes test efficiency and supports in-system test for long term reliability.

EDT Reduces Test Time and Pattern Volume without Sacrificing Coverage
The patented and award-winning Embedded Deterministic Test (EDT™) technology inserted into the design by TestKompress reduces both test time and pattern volume often by several orders of magnitude without any loss in fault coverage. The main components of EDT logic (decompressor and compactor) are part of the scan path only, so functional timing closure is not affected. EDT logic can be inserted in the RTL design, is ECO friendly, and is independent of design flows and synthesis tools. The EDT logic can be added at the top level of the design or used in a modular configuration by placing the decompressor and compactor into each block of the design. The EDT logic can also be incorporated into scan-isolated cores as part of a hierarchical DFT strategy.

Additional test cost reduction can be achieved using EDT Test Points generated by Tessent ScanPro. Unlike traditional test points used to increase random pattern testability, EDT Test Points use a novel algorithm to reduce ATPG pattern count by 2X to 4X for all fault models. For designs using modular EDT, scan input channels can be shared to improve compression up to 2X. For designs with multiple identical cores, compression can be improved up to 2X by broadcasting the scan input channels data.

FEATURES:
- Extensive fault model support, including stuck-at, transition, cell-aware, N-detect, timing-aware, bridge, IDDQ, path-delay, and user-defined.
- EDT technology reduces tester time and data volume
- Additional 2X-4X compression can be achieved using EDT Test Points generated by Tessent ScanPro.
- Channel sharing to non-identical cores provides up to 2X additional compression.
- Broadcasting scan data improves compression up to 2X for designs with identical cores.
- Supports low pin count test strategies (as few as one scan channel).
- Supports hierarchical test and pattern re-use, reducing test generation time, memory footprint, and pattern count for large designs.
- Support for a wide range of on-chip PLL/OCC implementations for at-speed test.
- Direct diagnosis of compressed patterns. Diagnosis-driven yield analysis with Tessent Diagnosis and Tessent YieldInsight.

BENEFITS:
- Accelerates failure analysis
- Highest test quality with the lowest test cost.
- Multi-processor pattern generation.
- Mentor Graphics award-winning customer support and consulting services ensure success.

www.mentor.com/Tessent
Hierarchical Test for Large Designs

Tessent TestKompress supports a hierarchical ATPG methodology that addresses many issues encountered when generating tests for large SoCs. A divide and conquer approach is used to reduce the overall ATPG task into smaller, more manageable pieces. Compressed patterns are first generated for each design core in isolation. These patterns are then automatically retargeted to the chip level and merged to minimize test time. Compressed patterns are then generated for top-level interconnect and glue logic.

This hierarchical approach typically results in 5X-10X reduction of ATPG runtime and memory footprint compared to running ATPG at the chip level. Pattern count (and consequently test time) is reduced by up to to 2x. Automation and dedicated design rule checks ensure safe and effective mapping of block core information to the top level. The hierarchical methodology removes DFT from the critical path to tapeout by allowing DFT and ATPG to be completed earlier in the design cycle.

Highest Defect Coverage

Tessent TestKompress supports all traditional fault models used for uncovering both static and dynamically activated defects. Support for user-defined fault models (UDFM) also allows virtually any defect mechanism to be modeled and targeted. TestKompress supports accurate at-speed clock edges and both launch-off-shift and capture transition fault application.

TestKompress supports an advanced test methodology called Cell-Aware Test that defines and uses fault models that target cell-internal defects. Cell-Aware test targets shorts, opens, and transistor defects internal to each standard cell, resulting in significant reductions in defective part (DPM) levels.

Productivity

Tessent TestKompress is built on the Tessent Shell platform, which offers comprehensive automation, TCL-based scripting, and introspection capabilities. To maximize throughput, ATPG can be distributed across multiple processors.

Tessent DFTVisualizer™ is integrated within Tessent TestKompress for viewing and correcting testability problems. DFTVisualizer presents the design, fault detection data, and any testability issues through various graphical interfaces to simplify design viewing and troubleshooting.

DFTVisualizer also provides automated analysis and visualization of design rule violations in order to present and highlight the most relevant information with minimal user effort. Comprehensive fault statistics reporting easily identifies sources of test coverage loss.

Mentor’s DFT and Yield Analysis Solutions

Tessent TestKompress is part of Mentor’s industry- and technology-leading tool suite for IC test and yield analysis. The Tessent product family includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on Linux.