Solutions for 2.5D and 3D Test
Tessent Support for Testing 3D-ICs

Challenges in Testing 3D IC Designs
The next phase of semiconductor designs will include the adoption of 3D IC packages. These vertical stacks of multiple bare die connected directly with through-silicon vias (TSVs) present three new test challenges to the industry:

■ Managing the escape rate of defective die at wafer to meet target post-packaging yield.
■ Testing stacked memory configurations.
■ Testing stacked logic configurations.
■ Comprehensive Solutions for Known Good Die

Achieving acceptable 3D IC package yield levels requires high-quality and cost-effective test at wafer sort. The Tessent® family of products provide innovative capabilities that address the known-good-die (KGD) testing challenges.

Probing limitations during wafer test typically result in limited IO testing. This is having a growing effect on bare die quality as the count and operating frequencies of IOs continue to increase. The Tessent Contactless IO test solution eliminates the wafer probing constraints while providing comprehensive test of static and leakage-related IO defects. In addition, Tessent SerdesTest also provides for the contactless test of high-speed SerDes IOs. Highly accurate testing of key parameters such as jitter and duty cycle are achieved using a fully embedded approach.

Significant reduction in die defect-per-million (DPM) levels can also be achieved with the Tessent Cell-Aware Test solution. Cell-Aware Test is a transistor-level test methodology that overcomes the limits of traditional stuck-at and transition fault models and associated test patterns by targeting specific shorts, opens, and transistor defects internal to each standard cell.

Testing Stacked Memories
Tessent MemoryBIST supports the test and diagnosis of memory die stacked on top of a silicon interposer or directly on top of a logic die. A BIST engine is integrated into the logic die and communicates to the TSV-based memory bus...
that connects the logic die to the memories. The BIST engine provides comprehensive at-speed testing of both the memory die and the memory bus connections.

The Tessent BIST engine communicates to a memory bus rather than directly to individual memories. This lets the BIST engine test the functional interface logic and TSVs.

The 3D memory BIST solution is run-time programmable. Using only the standard IEEE 1149.1 JTAG test interface, the BIST engine can be programmed in silicon for different memory counts, types, and sizes. Because the BIST engine is embedded into the logic die and can’t be physically modified without a design re-spin, this adaptability is essential. With full programmability, no re-design is needed over time even as the logic die is stacked with different memories and memory configurations for different applications.

DRAM die that adhere to the popular JEDEC Wide IO standard contain a scan chain on the DRAM’s IOs for supporting scan-based testing of the interconnect lines on these IOs. As part of the TSMC CoWoS flow, Tessent provides a feature for direct testing of the memory TSV connections. This feature is based on standard boundary scan and interfaces to the available JEDEC IO scan chain. The boundary scan approach however, only provides static testing of the TSV connections alone.

Testing Stacked Logic Die

Testing stacked logic die requires a way to access the DFT resources of each die in the stack. Tessent inserts an UTAG-based DFT interface, which includes a scan switch network for applying embedded compression test of each die and cascading 1149.1 TAPS across all die. This allows routing of control and test data through the stack to any of the die. The test data includes both 1149.1-based serial data as well as any scan-based data, such as compressed ATPG patterns. Scan patterns can be automatically retargetted from die-level to any position in the stack without additional pattern generation or the need for a complete netlist.

Testing the TSV connections between two stacked logic die is done through the use of standard 1149.1 boundary scan. Boundary scan cells are automatically inserted at each TSV in much the same way as for regular IO pads. Boundary scan patterns are then generated to target shorts and opens in the TSV interconnect.

Tessent Silicon Test and Yield Analysis Solutions

The Tessent family of products represents Mentor’s industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. These tools together provide the highest quality and most economical 3D-IC testing available. All Tessent tools are available on Linux. 

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