Need a Silicon Test Solution with Built-In Flexibility?

The Tessent® product family is a comprehensive silicon test and yield analysis solution that addresses the challenges of manufacturing test, debug, and yield ramp for today’s SOCs. Built on the foundation of the best-in-class solutions for each test discipline, Tessent brings them together in a powerful test flow that ensures total chip coverage.

The flexibility of the Tessent product family enables high-quality tests to be applied throughout the product lifecycle—from wafer and package test to burn-in, in-system, and field test. Accurate yield analysis is achieved by exploiting the structural nature of scan test and BIST methodologies and correlating to physical features.

The full Tessent product family combines deterministic scan testing, embedded pattern compression, built-in self test, specialized embedded memory test and repair, boundary scan, mixed-signal test, and silicon learning technologies.

Contact Tessent@mentor.com

The Comprehensive Tessent Product Family

**Scaling**
- Tessent TestKompress®
- Tessent Scan
- Tessent ScanPro
- Tessent FastScan™
- Tessent BoundaryScan
- Tessent IJTAG
- Tessent DesignEditor

**Automotive**
- Tessent MissionMode
- Tessent LogicBIST
- Tessent MemoryBIST
- Tessent DefectSim
- Tessent CellModelGen Plus

**Silicon Learning**
- Tessent Diagnosis
- Tessent YieldInsight®
- Tessent SiliconInsight®
Tessent Design-for-Test

The Tessent product family includes the industry’s most powerful solutions for logic, memory, and mixed-signal test. Tessent tools are time and tape-out proven to deliver high-quality test using both compression and vectorless approaches. They provide the maximum flexibility for achieving the most effective test cost versus quality optimization.

Scaling

**Tessent TestKompress** automatic test pattern generation (ATPG) delivers the highest quality scan test with the lowest manufacturing test cost. Its industry-proven ATPG engine offers 100x or better test compression and targets all the fault models necessary for thorough silicon test.

The industry-proven Cell-aware capability in Tessent TestKompress targets transistor-level defects to significantly improve product quality.

**Tessent ScanPro** includes VersaPoint™ technology, a single test point solution for ATPG and LBIST, which improves compression by 2x to 4x for all fault models. Tessent Scan and ScanPro are the industry’s highest capacity and most flexible scan test solutions, and facilitate hierarchical DFT with advanced wrapper analysis.

Hierarchical test is supported through wrapper insertion and retargeting of scan patterns from block level to chip level for effective test reuse. With hierarchical test, ATPG and diagnosis tool runtime and compute resources are reduced by 10x and pattern count by 2x.

**Tessent JTAG** supports the IEEE 1687 standard for plug-and-play IP integration. It helps you connect any number of IEEE 1687 compliant IP blocks into an integrated, hierarchical network and to communicate commands to the blocks from a single top-level access point.

**Automotive**

All Tessent tools are ISO 26262 qualified and support the quality and reliability requirements of ICs for automotive applications.

**Tessent MissionMode** provides IP and automation to test and diagnosis ICs in an automotive system at any time during a vehicle’s operation.

**Tessent LogicBIST** provides complete core-level test handoff for in-system test or test through a limited tester interface such as for burn-in board test and multi-chip module (MCM). Tessent TestKompress and LogicBIST can be used together in a hybrid approach that shares test logic.

**Tessent MemoryBIST** provides at-speed testing, diagnosis, and repair of embedded memories. The solution’s architecture is hierarchical, allowing BIST and self-repair capabilities to be added to individual cores as well as at the top level. Several new features enable efficient, low-latency in-system test and repair.

**Tessent DefectSim** is a transistor-level defect simulator for analog, mixed-signal (AMS), and non-scan digital circuits. It replaces manual test coverage assessment needed to meet quality standards such as ISO 26262. Tessent DefectSim is perfect for both high-volume and high-reliability ICs.