Test for Safety-Critical Applications

Tessent Hybrid TK/LBIST

Addressing Safety-Critical Test Requirements

Tessent® Hybrid TK/LBIST is a high-quality silicon test solution ideal for safety-critical applications such as ICs for use in the automotive and medical industries. The solution provides both highly efficient production test as well as support for in-system self-test necessary to meet the high quality and reliability requirements defined by standards such as ISO 26262.

Components of the Hybrid Solution

Although ATPG compression and logic BIST have historically been used independently and for different applications, they possess complementary features that turn out to be very beneficial in combination. Tessent Hybrid TK/LBIST takes advantage of many similarities between the two approaches to deliver a highly efficient combined solution. The solution shares on-chip DFT resources such as scan chains and clock control logic. Tessent TK/LBIST also combines the on-chip controller logic for both ATPG compression and logic BIST into a single block that is significantly smaller than the two separate implementations. The combined architecture provides the ability to apply any combination of compressed and random patterns.

A single automation flow based on Tessent Shell enables both a flat as well as hierarchical integration of the hybrid capabilities. The comprehensive flow includes advanced design rule checking, hybrid controller insertion and verification, flexible scan insertion, and fault simulation accumulated across both pattern types.

Maximum Test Efficiency

The table below compares the benefits of ATPG compression and logic BIST to those provided by the Hybrid TK/LBIST solution. One clear benefit of the hybrid solution is the increased test efficiency that is achieved by a combination of increased quality and reduced test time. Higher test quality is achieved through the combination of compressed patterns targeting

FEATURES:

- Single comprehensive automation flow for quick integration of all combined capabilities.
- Supports both a flat top-down or hierarchical bottom-up test integration flow.
- Hybrid on-chip logic provides combined set of test capabilities for a fraction of the combined area overhead.
- Supports run-time selection between random patterns and compressed pattern application.

BENEFITS:

- Highest test quality — Combination of compressed patterns targeting advanced fault models together with random patterns for coverage of un-modeled defects and high N-Detect results in highest manufacturing test quality.
- Shortest test time — High-bandwidth random pattern application together with potential for greater test parallelization across multiple cores results in minimum test times.
- Highest test efficiency — Use of VersaPoint test point technology for 2-4X reduction in ATPG pattern count and 2%-4% higher LBIST coverage.
- In-System Reliability — Supports high-quality in-field self-test for meeting reliability requirements imposed by standards such as ISO 26262.
- Superior support quality — Mentor Graphics has the only 5-Star support in EDA.

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advanced fault models together with random patterns for coverage of deterministic defects and high N-detect.

<table>
<thead>
<tr>
<th>Quality</th>
<th>Logic BIST</th>
<th>ATPG Compression</th>
<th>Hybrid TK/LBIST</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>High. Additional detection of un-modeled defects.</td>
<td>High. Additional detection with patterns for small delay, Cell-Aware, etc.</td>
<td>Highest.</td>
</tr>
<tr>
<td>Application Time</td>
<td>Short if design is not pseudo-random resistant.</td>
<td>Depends on the number of pattern sets desired.</td>
<td>Shortest. LBIST for quick detection and ATPG to ‘top-up’.</td>
</tr>
<tr>
<td>Environment</td>
<td>Minimal interface. Retest is system and burn-in.</td>
<td>Needs a tester.</td>
<td>All environments.</td>
</tr>
<tr>
<td>Target Design Type</td>
<td>Designs that need retest in system.</td>
<td>Any digital circuits.</td>
<td>Mission-critical chips, such as for automotive and medical.</td>
</tr>
</tbody>
</table>

Test time is reduced by the combination of LBIST’s quick detection of a large number of faults with the high-bandwidth application of random patterns followed by a much smaller set of compressed ATPG patterns to cover the remaining undetected faults. The hybrid solution can also reduce the total test time for a complex hierarchical design. Each core is equipped with its own hybrid test infrastructure, so each core can be tested independently of other cores. Full tester bandwidth can be used to more quickly apply compressed patterns to some cores while random patterns are applied to others and the process is then reversed, thus reducing overall test time.

**VersaPoint Test Point Technology**

Engineered for hybrid TK/LBIST applications, the Tessent VersaPoint™ test point technology improves ATPG pattern count and logic BIST testability at the same time. VersaPoint technology gives 2-4X reduction in ATPG pattern count compared to TestKompress alone, and LBIST coverage typically 2%-4% higher than when using traditional LBIST test points.

**Support for the ISO 26262 Standard**

The Tessent Hybrid TK/LBIST solution supports high-quality test in multiple environments. Both deterministic and random patterns can be used for manufacturing test. Random patterns can also be used in post-manufacturing environments such as burn-in, system-level test, and in-field self-test. The ability of a device to periodically test itself in the field is a necessity in many safety-critical applications, and is key to satisfying the reliability requirements specified within the ISO 26262 automotive safety standard. The hybrid controller is accessed along with other potential BIST capabilities through a standard IEEE 1687 network, allowing easier access to the embedded test capabilities from within the system.

**Mentor’s Silicon Test and Yield Analysis Solutions**

The Hybrid TK/LBIST solution requires both Tessent TestKompress and Tessent LogicBIST, which are part of Mentor’s industry- and technology-leading suite of silicon test and yield analysis products. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on RedHat and Suse Linux.