In-System Test and Diagnosis of Automotive ICs
Tessent MissionMode

Ensuring System Reliability with in-system Self-test
The Tessent MissionMode solution provides a combination of automation and on-chip IP for enabling semiconductor chips throughout an automotive electronics system to be tested and diagnosed at any point during a vehicle’s functional operation. This capability is a fundamental requirement for achieving the safety and long-term reliability requirements demanded by the ISO 26262 standard.

Flexible In-system Test Infrastructure
The Tessent MissionMode architecture provides system-level low latency access to all on-chip test resources for on-line test and diagnosis. An IEEE 1687 (IJTAG) based network is used to provide access to all of the test IP distributed throughout the design. The test IP can consist of any Tessent BIST of DFT capabilities (such as memory BIST, logic BIST, or EDT logic) or any 3rd party IJTAG-compliant IP. The hierarchical network of scan insertion bit (SIB) switches allows for versatile and efficient communication to the distributed test resources. An IEEE 1149.1 test access port (TAP) provides external access to the IJTAG network and is primarily used within the manufacturing test environment.

At the heart of this test architecture is the Tessent MissionMode controller, which can take over the TAP signals and drive any test or diagnostic commands to any and all of the test IP in the IJTAG network. One or more MissionMode controllers can also be configured to communicate directly to a single or small group of test IP. This configuration has the benefit of reducing the communication latency to the test IP, which can be critical for certain tests.

Real-time Test Control
The Tessent MissionMode controller can be configured to operate in two different modes. In CPU access mode, the controller supports parallel read and write operations to and from a CPU bus. The controller performs the

FEATURES:
• Provides CPU-based communication to all on-chip test resources.
• Supports communication and control of any IJTAG-compliant IP.
• Fully automated infrastructure integration and verification flow.
• Automated translation between IJTAG serial data and parallel CPU read/write commands.

BENEFITS:
• Helps meet safety and reliability requirements imposed by the ISO 26262 standard.
• Eliminates the cost and time associated with developing ad-hoc in-system test access capabilities.
• Improves work efficiency through seamless integration with all Tessent BIST and DFT capabilities.
• Mentor Graphics award-winning customer support ensures success.

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parallel-to-serial and serial-to-parallel data conversion necessary to transport information between the CPU bus and the UJTAG network. This mode supports a system-level communication architecture based on a backplane bus. A service processor can access each Tessent MissionMode controller and hence any on-chip test IP through any vehicle bus such as Controller Area Network (CAN) or Inter-Integrated Chip (I2C).

In the direct memory access (DMA) mode, the Tessent MissionMode controller reads command data preloaded in a non-volatile memory such as a ROM. Multiple test sequences can be stored and subsequently retrieved in any order and as many times as desired during system operation. This not only provides the flexibility to run different tests at different times, but also allows longer tests to be broken into smaller segments and applied at different intervals.

Tessent MissionMode automates the integration and full verification of the UJTAG infrastructure and also automates the generation of all CPU instructions necessary to run any tests and extract any diagnostic results.

Support for ISO 26262 ASIL Certification
Each Tessent MissionMode software release is delivered with an ISO 26262 software tool qualification report that provides the required evidence of the tool's suitability for ISO 26262 related tasks. The report can be used to simplify the ASIL device certification process significantly. All Tessent software tool qualification reports are certified by SGS-TüV Saar.

Tessent DFT and Yield Analysis Solutions
Tessent MissionMode is part of the Mentor industry- and technology-leading tool suite for DFT and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis.

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